

DATA SHEET



PCF8813

**(67 + 1) × 102 pixels matrix LCD
driver**

Product specification
Supersedes data of 2002 Sep 24

2004 Mar 05

(67 + 1) × 102 pixels matrix LCD driver**PCF8813**

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(67 + 1) × 102 pixels matrix LCD driver**PCF8813****1 FEATURES**

- Single-chip LCD controller or driver
- 67 row + 1 icon row, 102 column outputs (the icon row is available twice to allow icons to be displayed at the top or at the bottom of the display)
- Very low power consumption, optimized for battery operated systems
- On-chip:
 - Display data RAM 68 × 102 bits
 - Configurable voltage multiplier (× 5, × 4, × 3 and × 2) generating highly accurate V_{LCD} and includes booster capacitors (external V_{LCD} is also possible)
 - Temperature compensation of V_{LCD} with four selectable temperature coefficients
 - Generation of intermediate LCD bias voltages
 - Highly-accurate built-in oscillator requiring no external components (an external clock is also possible)
- High integration level resulting in minimum number of external capacitors and resistors
- Selectable 8-bit parallel interface, 3-line or 4-line Serial Peripheral Interface (SPI), 3-line serial interface and high-speed I²C-bus interface
- External reset input
- CMOS compatible inputs
- Mux rates: 1 : 9 to 1 : 65 in steps of 8 and 1 : 68
- Logic supply voltage range 1.7 to 3.3 V
- High voltage generator supply voltage range 2.4 to 4.5 V
- Display supply voltage range 3.0 to 9.0 V
- One Time Programmable (OTP) V_{LCD} trimming
- Horizontal and vertical mirroring
- Status read which allows chip recognition and content checking of some registers



- Start address line which allows, for instance, scrolling of the displayed image
- Programmable display RAM pointers for various display sizes
- Slim chip layout optimized for chip-on-glass applications
- Operating temperature range –40 to +85 °C
- Very close tolerance on V_{LCD} and frame frequency for excellent optical performance
- Support for LCD cell tolerance compensation of V_{LCD} by OTP storage.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

3 GENERAL DESCRIPTION

The PCF8813 is a low power CMOS LCD controller driver designed to drive a graphic display of 67 rows and 102 columns plus an icon row of up to 102 symbols. All necessary functions for the display are provided in a single chip, including on-chip generation of the LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8813 can interface to microcontrollers via a parallel, serial or I²C-bus interface.

4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|----------------|---------|---------------------------------|---------|
| | NAME | DESCRIPTION | VERSION |
| PCF8813U/2DA/2 | – | chip with bumps in tray for COG | – |

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5 BLOCK DIAGRAM

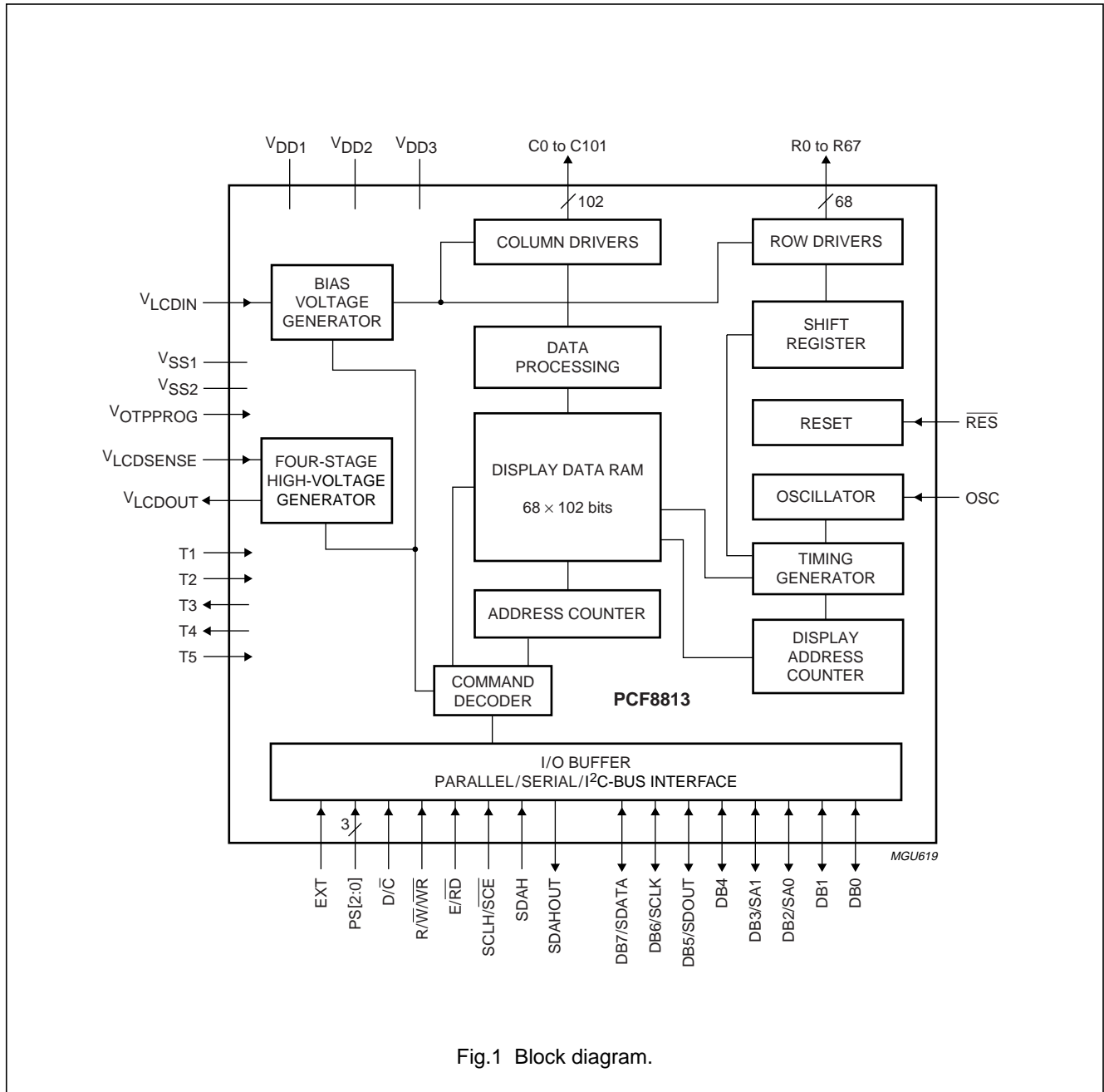


Fig.1 Block diagram.

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6 PINNING

| SYMBOL | PAD ⁽¹⁾ | DESCRIPTION |
|----------------------|--------------------|--|
| R15 to R0 | 7 to 22 | LCD row driver outputs |
| R16 to R31 | 23 to 38 | |
| C0 to C101 | 39 to 140 | LCD column driver outputs |
| R67 | 141 | LCD row driver output for row 67 (used only for icons) |
| R66 to R48 | 142 to 160 | LCD row driver outputs |
| R32 to R47 | 161 to 176 | |
| R67 | 177 | duplicated LCD row driver output for row 67 (used only for icons) |
| SDAHOUT | 183 | data output for I ² C-bus interface; notes 2 and 3 |
| SDAH | 184 to 185 | data output for I ² C-bus interface; note 2 |
| V _{DD1} | 186 to 191 | supply voltage 1; note 4 |
| V _{DD3} | 192 to 196 | supply voltage 3; note 4 |
| V _{DD2} | 197 to 206 | supply voltage 2; note 4 |
| V _{DD1} | 207 | supply voltage 1; notes 4 and 5 |
| R/W/WR | 208 | READ/WRITE (6800) or WRITE (8080 interface) input; note 6 |
| E/RD | 209 | clock enable (6800 interface) or READ (8080 interface) input; note 7 |
| DB0 | 210 | parallel data input/output; note 8 |
| DB1 | 211 | parallel data input/output; note 8 |
| DB2/SA0 | 212 | parallel data input/output or I ² C-bus slave address input (bit 0) |
| DB3/SA1 | 213 | parallel data input/output or I ² C-bus slave address input (bit 1) |
| DB4 | 214 | parallel data input/output; note 8 |
| DB5/SDOUT | 215 | parallel data input/output or serial output (SDOUT) |
| DB6/SCLK | 216 | parallel data input/output or output or serial clock input (SCLK) |
| DB7/SDATA | 217 | parallel data input/output or serial data input (SDATA) |
| V _{SS1} | 218 | ground voltage 1; notes 5 and 9 |
| D/C | 219 | data/command; note 10 |
| SCE/SCLH | 220 to 221 | chip enable or clock input for I ² C-bus interface |
| V _{OTPPROG} | 222 to 224 | voltage inputs for OTP programming; see note 11 |
| V _{DD1} | 225 | supply voltage 1; notes 4 and 5 |
| OSC | 226 | oscillator input; note 12 |
| V _{SS2} | 227 to 236 | ground voltage 2; note 9 |
| V _{SS1} | 237 to 246 | ground voltage 1; note 9 |
| T5 | 247 | test input 5; note 13 |
| T1 | 248 | test input 1; note 13 |
| T2 | 249 | test input 2; note 13 |
| PS0 | 250 | parallel/serial/I ² C-bus data input selection pad 0 |
| PS1 | 251 | parallel/serial/I ² C-bus data input selection pad 1 |
| PS2 | 252 | parallel/serial/I ² C-bus data input selection pad 2 |
| V _{DD1} | 253 | supply voltage 1; notes 4 and 5 |
| T4 | 254 | test output 4; note 13 |
| T3 | 255 | test output 3; note 13 |

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| SYMBOL | PAD ⁽¹⁾ | DESCRIPTION |
|-----------------------|--------------------|--|
| V _{LCDIN} | 256 to 262 | LCD supply voltage input; note 14 |
| V _{LCDOUT} | 263 to 271 | generated LCD supply voltage; note 14 |
| V _{LCDSENSE} | 272 | voltage multiplier (V _{LCD}) regulation input; note 14 |
| RES | 273 | external reset input |

Notes

- Dummy pads are located at positions 1, 2, 3, 5, 6, 179, 180, 181, 182 and 274; dummy and alignment pads are located at positions 4 and 178.
- When not in use, this pad must be connected to V_{DD1} or V_{SS1}.
- Output SDAHOUT is used as the data acknowledge output when the I²C-bus is selected. By connecting SDAHOUT to SDAH externally, the SDAH line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in COG applications because where the track resistance from the SDAHOUT pad to the SDAH line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. Therefore it is possible during the acknowledge cycle that the PCF8813 will not create a logic LOW level. By splitting the SDAH input from the SDAHOUT output, the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAHOUT pad to the system SDAH line to guarantee a valid LOW level.
- V_{DD2} and V_{DD3} supply the internal voltage generator, both have the same voltage and may be connected together outside of the chip; V_{DD1} supplies the remainder of the chip. V_{DD1}, V_{DD2} and V_{DD3} can be connected together but then care must be taken with respect to the supply voltage range. If the internal voltage generator is not used, pads V_{DD2} and V_{DD3} must be connected to pads V_{DD1}.
- This pad can be used to tie-off unused input pads to the power supply voltage or to ground.
- This input is not used in serial and I²C-bus mode and must therefore be connected to either V_{DD1} or V_{SS1}.
- This input is not used when the serial or I²C-bus interface is selected and must therefore be connected to V_{DD1} or V_{SS1}.
- When serial or I²C-bus mode is selected, the unused parallel pads must be connected to V_{DD1} or V_{SS1}.
- Supply rails V_{SS1} and V_{SS2} must be connected together.
- This input is not used with the 3-line serial interface and must therefore be connected to V_{DD1} or V_{SS1}.
- This pad can be connected externally to the $\overline{\text{SCE}}/\text{SCLH}$ pad to reduce the number of pads routed in COG applications. When not connected in this configuration, V_{OTPPROG} must be connected to either V_{DD1} or V_{SS1} after completion of OTP programming and after the seal bit has been set.
- When the on-chip oscillator is used, the OSC input must be connected to V_{DD1}. If an external clock signal is used, then this is connected to the OSC input. If both the oscillator and external clock are inhibited by connecting pad OSC to V_{SS1}, the display is not clocked and may be in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.
- Test pads T1 to T5 are not accessible to users: T1, T2 and T5 must be connected to V_{SS}; T3 and T4 must be open-circuit.
- Positive power supply for the liquid crystal display (see also Figs 51, 52 and 53):
 - If the internal voltage generator is used, pads V_{LCDIN}, V_{LCDSENSE} and V_{LCDOUT} must be connected together.
 - An external LCD supply voltage can be supplied using the V_{LCDIN} pad, this requires that pad V_{LCDOUT} is open-circuit, pad V_{LCDSENSE} is connected to the V_{LCDIN} input, and the internal voltage generator is switched off. In Power-down mode, the external LCD supply voltage must be switched off.

(67 + 1) × 102 pixels matrix LCD driver**PCF8813****7 FUNCTIONAL DESCRIPTION****7.1 I/O buffer and interface**

One of five industrial standard interfaces can be selected using the interface configuration inputs PS2, PS1 and PS0.

Table 1 Parallel/serial/I²C-bus interface selection

| PS2 | PS1 | PS0 | INTERFACE |
|-----|-----|-----|---|
| 0 | 0 | 0 | 3-line SPI |
| 0 | 0 | 1 | 4-line SPI |
| 0 | 1 | 0 | 8080 parallel interface |
| 0 | 1 | 1 | 6800 parallel interface |
| 1 | 0 | 0 | high-speed I ² C-bus interface |
| 1 | 1 | 0 | |
| 1 | 0 | 1 | 3-line serial interface |
| 1 | 1 | 1 | |

7.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. An external clock signal, if used, is connected to this input.

7.3 Address counter

The Address Counter (AC) assigns addresses to the display data RAM for writing. The X address X[6:0] and the Y address Y[3:0] are set separately.

7.4 Display data RAM

The PCF8813 contains a 68 × 102 bit static RAM which stores the display data. The Display Data RAM (DDRAM) is divided into eight banks of 102 bytes (8 × 8 × 102 bits), one bank of 1 × 3 × 102 bits and a separate bank of 1 × 1 × 102 for icons. During RAM access, data is transferred to the RAM via any of the four interfaces. There is a direct correspondence between the X address and the column output number.

7.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data buses.

7.6 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The display status (all dots on/off and normal/inverse video) is set by bits D and E in the display control command.

7.7 LCD row and column drivers

The PCF8813 contains 68 row and 102 column drivers, which connect the appropriate LCD bias voltages in a sequence to the display in accordance with the data that is to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.

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7.8 LCD waveforms and DDRAM to data mapping

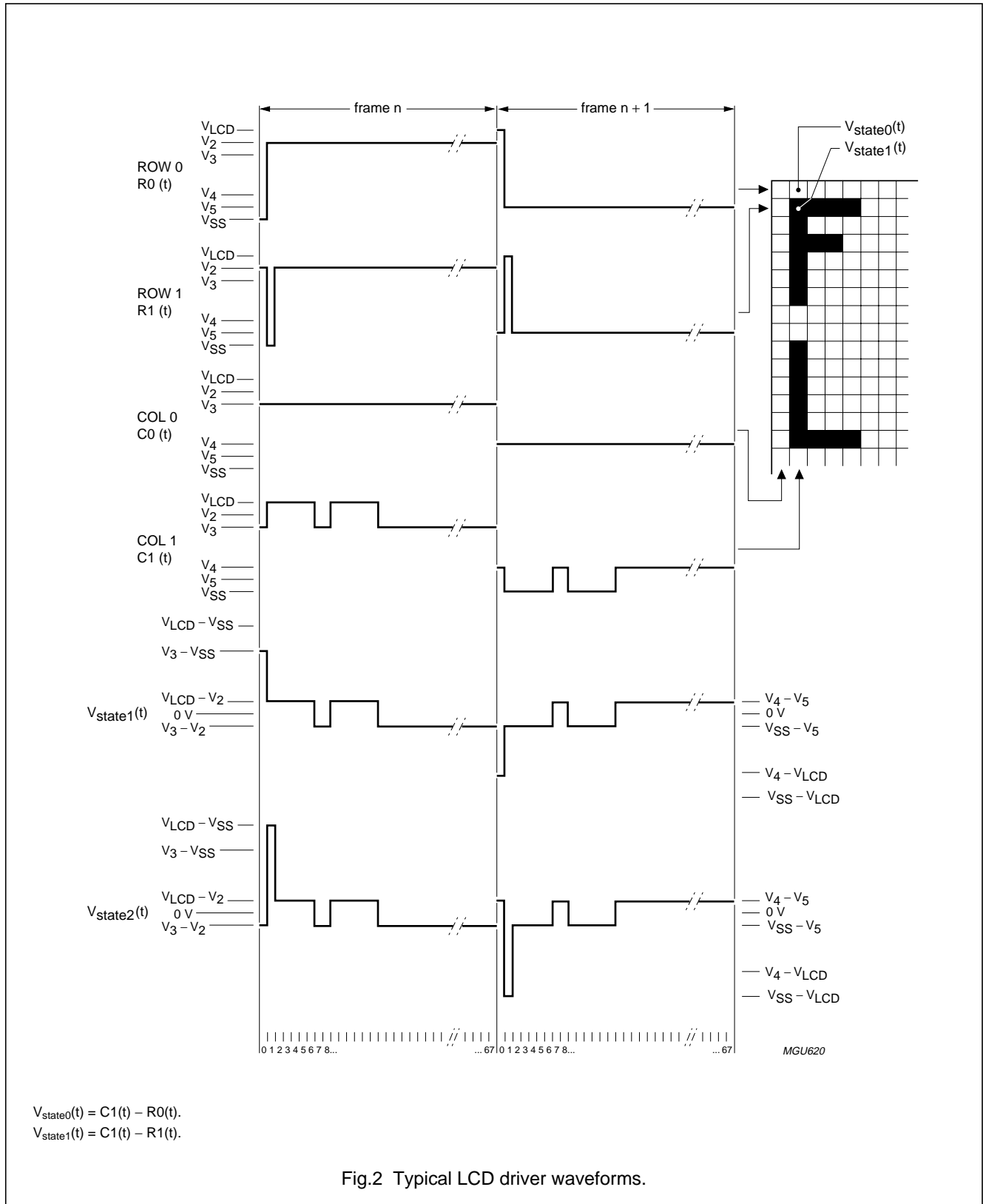


Fig.2 Typical LCD driver waveforms.

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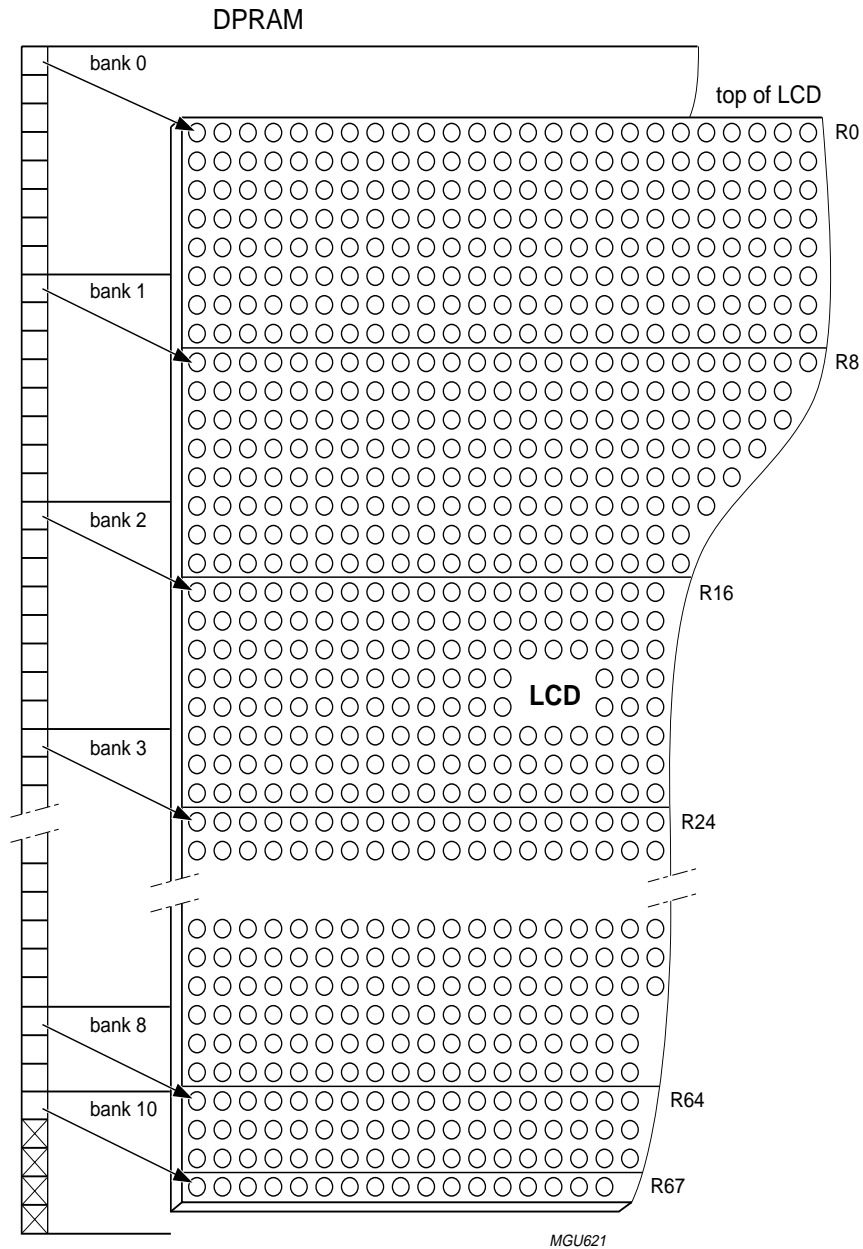


Fig.3 Display data RAM.

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7.9 DDRAM addressing

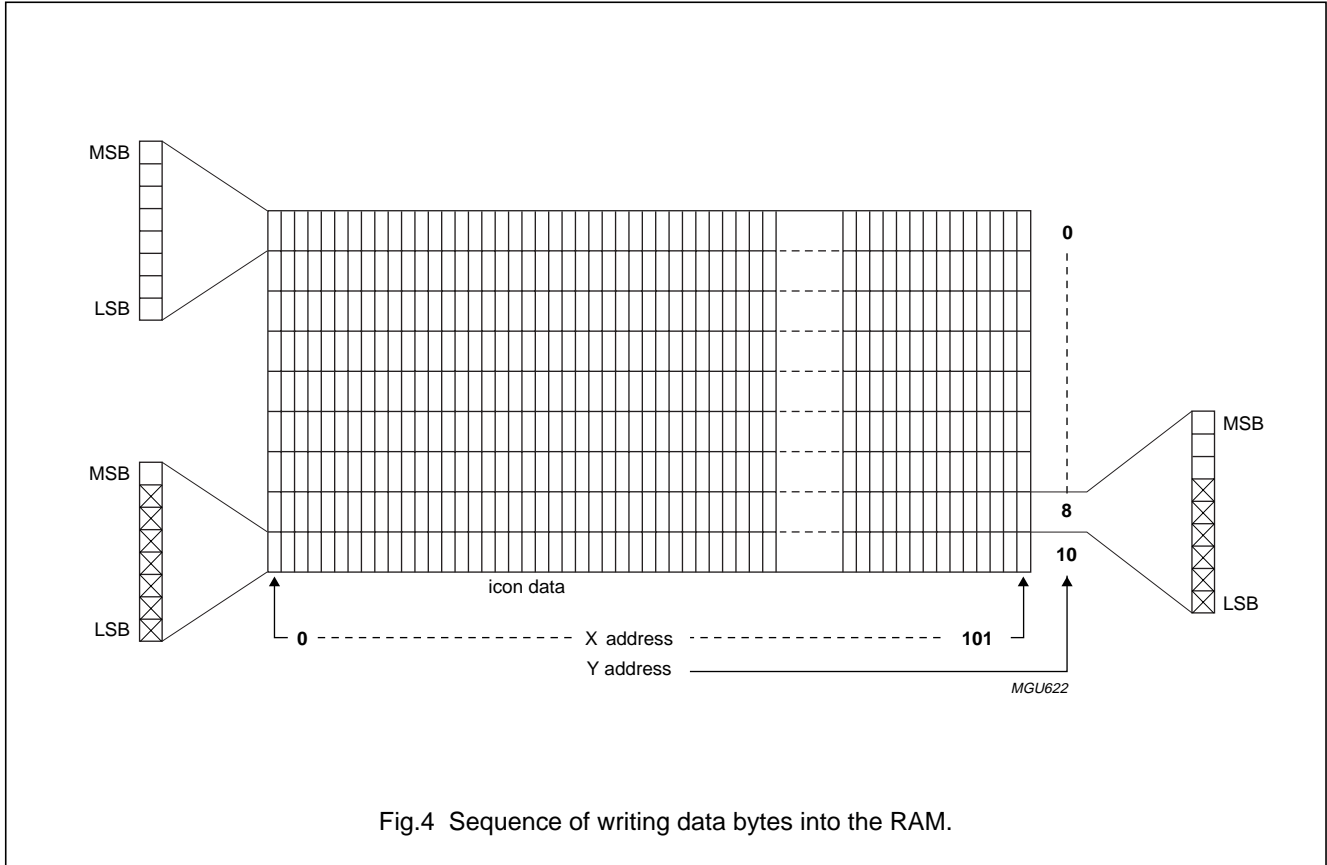


Fig.4 Sequence of writing data bytes into the RAM.

Data is downloaded in bytes into the RAM matrix of the PCF8813 as indicated in Fig.4. The display data RAM has a matrix of 68 by 102 bits. The columns are addressed by the X address pointer whilst the rows are addressed in groups of 8 by the Y address pointer. However, there are only three rows in bank 8 and one row in bank 10. There is no bank 9. Thus the address ranges are: X = 0 to 101 (1100101) and Y = 0 to 8 and then 10 (1010). The PCF8813 is limited to 102 columns by 68 rows, addressing the RAM outside this area is not allowed.

Two different addressing modes are possible; horizontal addressing and vertical addressing.

In the horizontal addressing mode (V = 0) the X address increments after each byte. After the last X address (X = 101), x wraps-around to 0 and Y increments to address the next row (see Fig.5) until bank 8 is filled. In the vertical addressing mode (V = 1) the Y address increments after each byte. After the Y address (Y = 8), there is Y wraparound to 0 and X increments to address the next column (see Fig.6). After the very last address (X = 101 and Y = 8) the address pointers wraparound to address X = 0 and Y = 0 in both addressing modes.

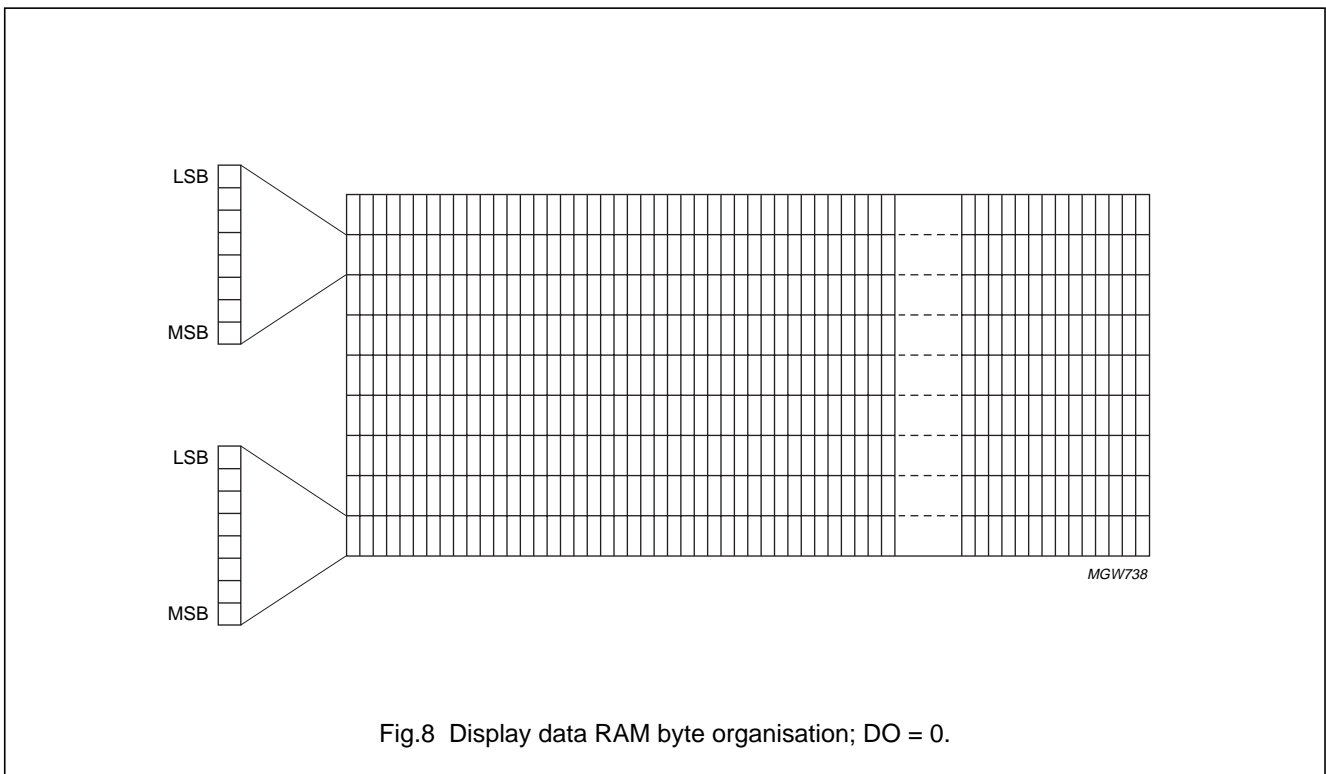
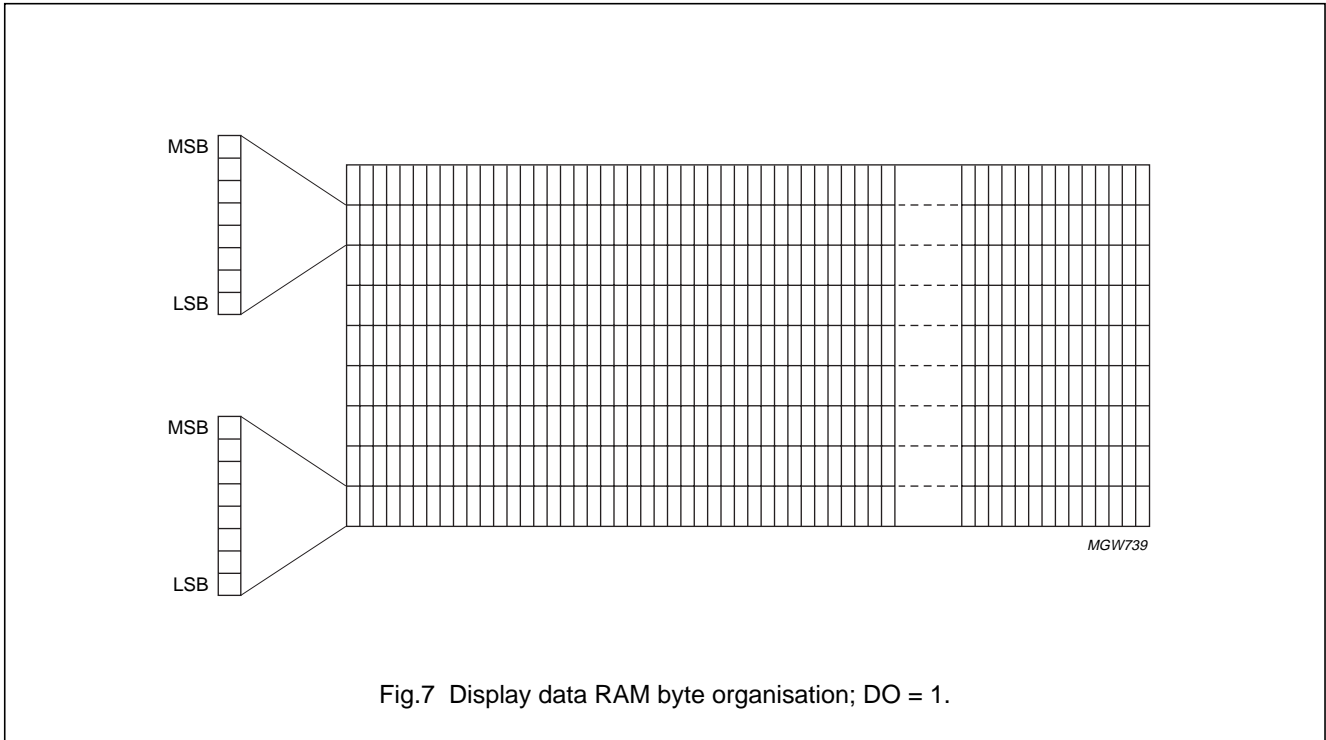
Addressing in bank 10 is a special case as these RAM locations are not automatically accessed. Bank 10 is reserved for icons. Icon locations must be addressed explicitly by setting the Y address pointer to 10. The Y address pointer does not auto-increment when the X address overflows or underflows (it stays in set to bank 9). Writing icon data is independent of the horizontal or vertical addressing (V-bit) but is affected by the Mirror X (MX) and Mirror Y (MY) bits. MX and MY are described in Sections 7.11 and 7.12.

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7.10 Data order

The Data Order bit (DO) defines the bit order (MSB on top or LSB on top) for writing in the RAM; see Figs 7 and 8.

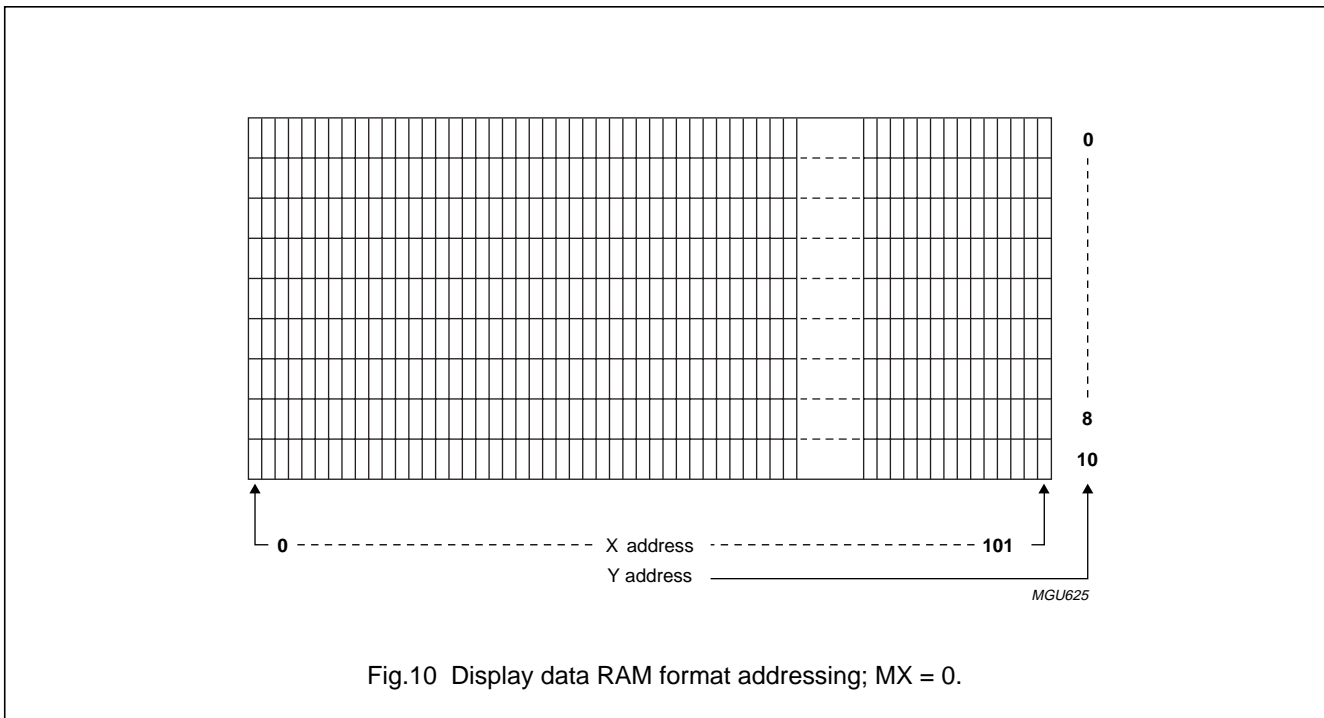
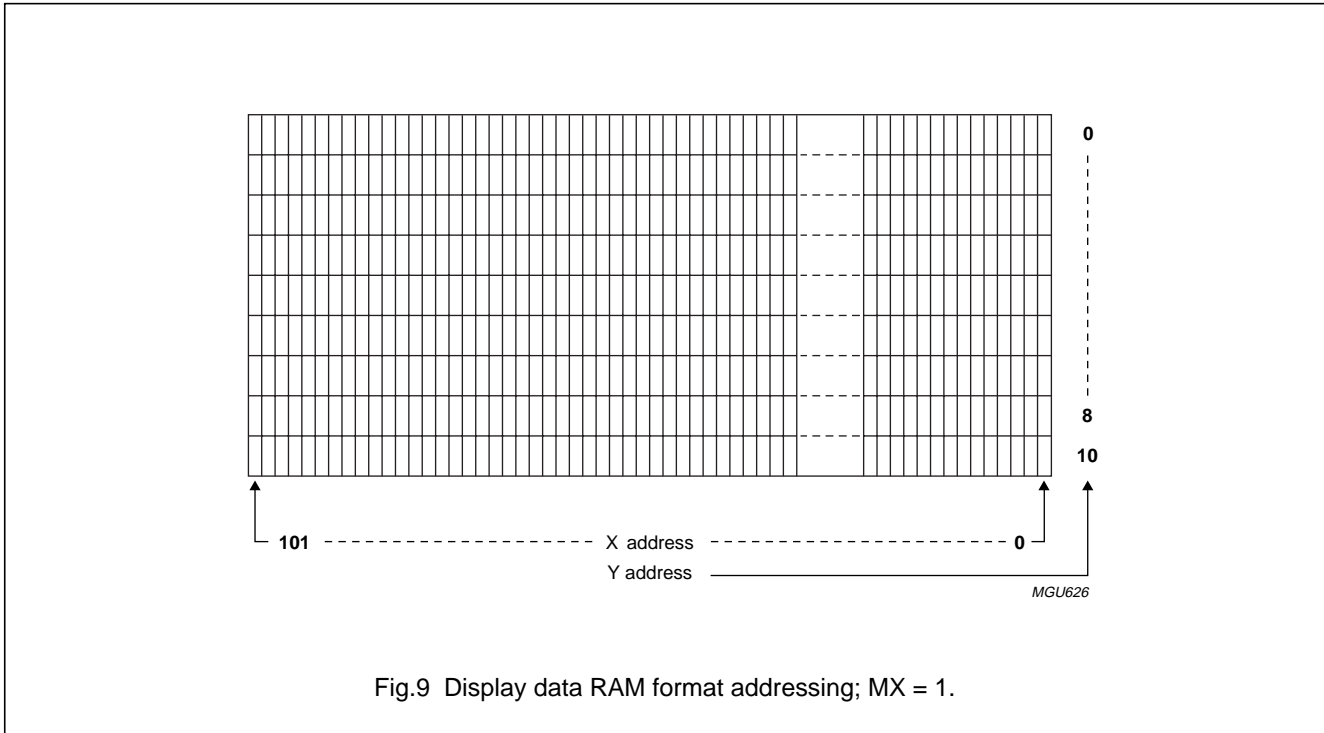


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7.11 Mirror X

The MX bit allows horizontal mirroring. When $MX = 1$, the X address space is mirrored (see Fig.9). The address $X = 0$ is then located at the right side (column 101) of the display. When $MX = 0$, mirroring is disabled and the address $X = 0$ is located at the left side (column 0) of the display (see Fig.10).

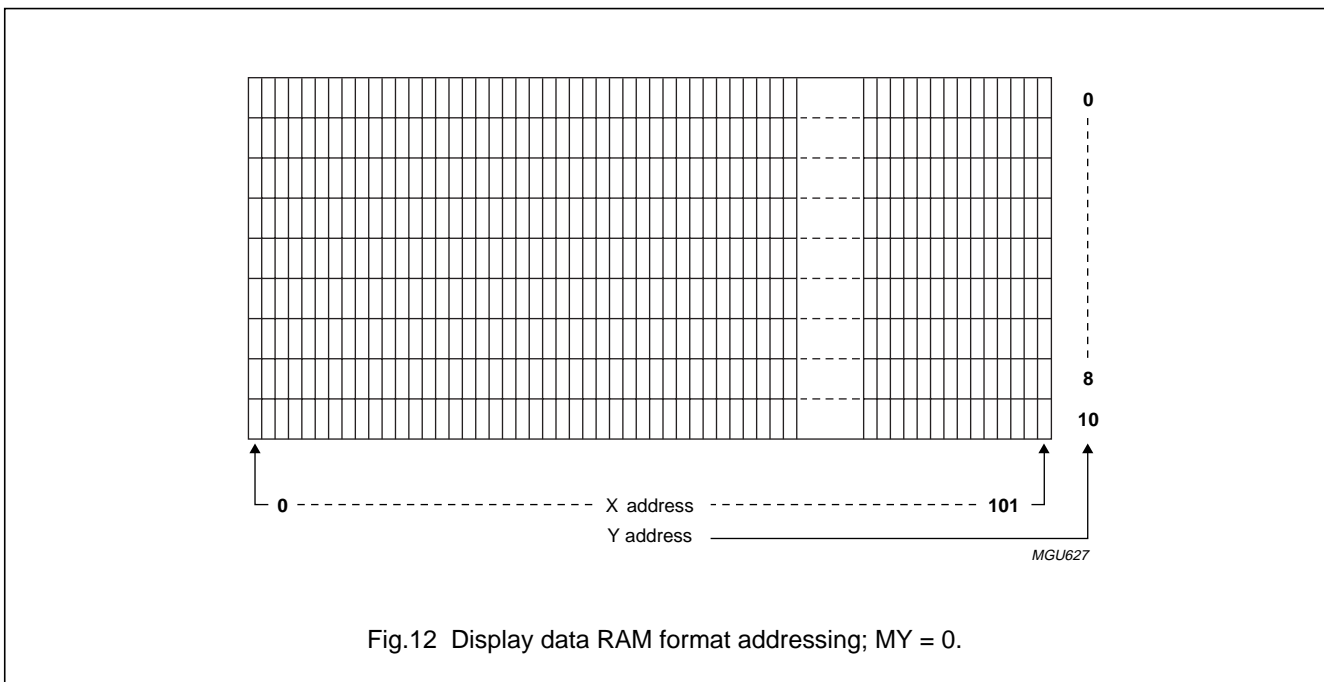
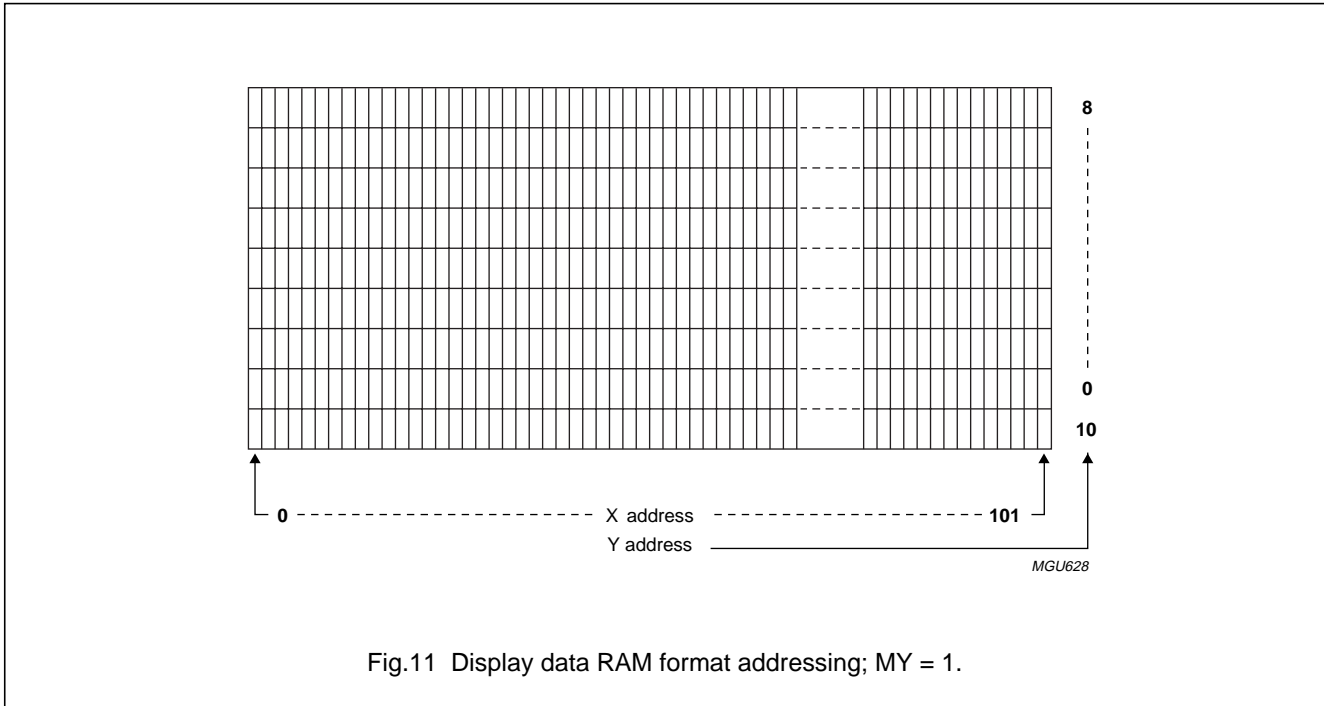


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7.12 Mirror Y

The MY bit allows vertical mirroring. When MY = 1, the Y address space is mirrored resulting in an upside-down display. The address Y = 0 is then located at the bottom of the display (see Fig.11). When MY = 0, the mirroring is disabled and the address Y = 0 is located at top of the display (see Fig.12). A change in the state of MY has an immediate effect on the display and the effect of MY is visible immediately the bit is modified. This feature makes it possible to mount the device at the top or bottom of the display.



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7.13 Bottom row swap

This mode swaps the order of the order of the rows; see Figs 13 and 14. The mode is useful to aide routing to displays when it is not possible to pass tracks under the device, as in the case of Tape Carrier Packages (TCP).

7.14 Output row order

The order in which the rows are activated is a function of bits Bottom Row Swap (BRS), Mirror Y (MY) and Normal Partial mode (N/P). This has important implications when the device is used either in COG or TCP applications.

When MY is set to 0, the RAM is accessed in a linear manner, starting at R0, counting to R66, then jumping to

the end for the icon data. When MY is set to 1, the RAM is still accessed in a linear manner but starting from the last row, counting down to zero and then jumping to the icon data.

When N/P is set to 1, the Free Programmable Mux Rate (FPMR) mode is disabled and row addressing is in normal mode (see Section 11.9), therefore counting is the same as for MY = 0 and BRS = 0. When N/P is 0, FPMR mode is enabled. Only 65 rows are addressed/read in FPMR mode.

Figures 13 and 14 show the possibility of connecting the icon row (row R67) at the top or bottom of the display.

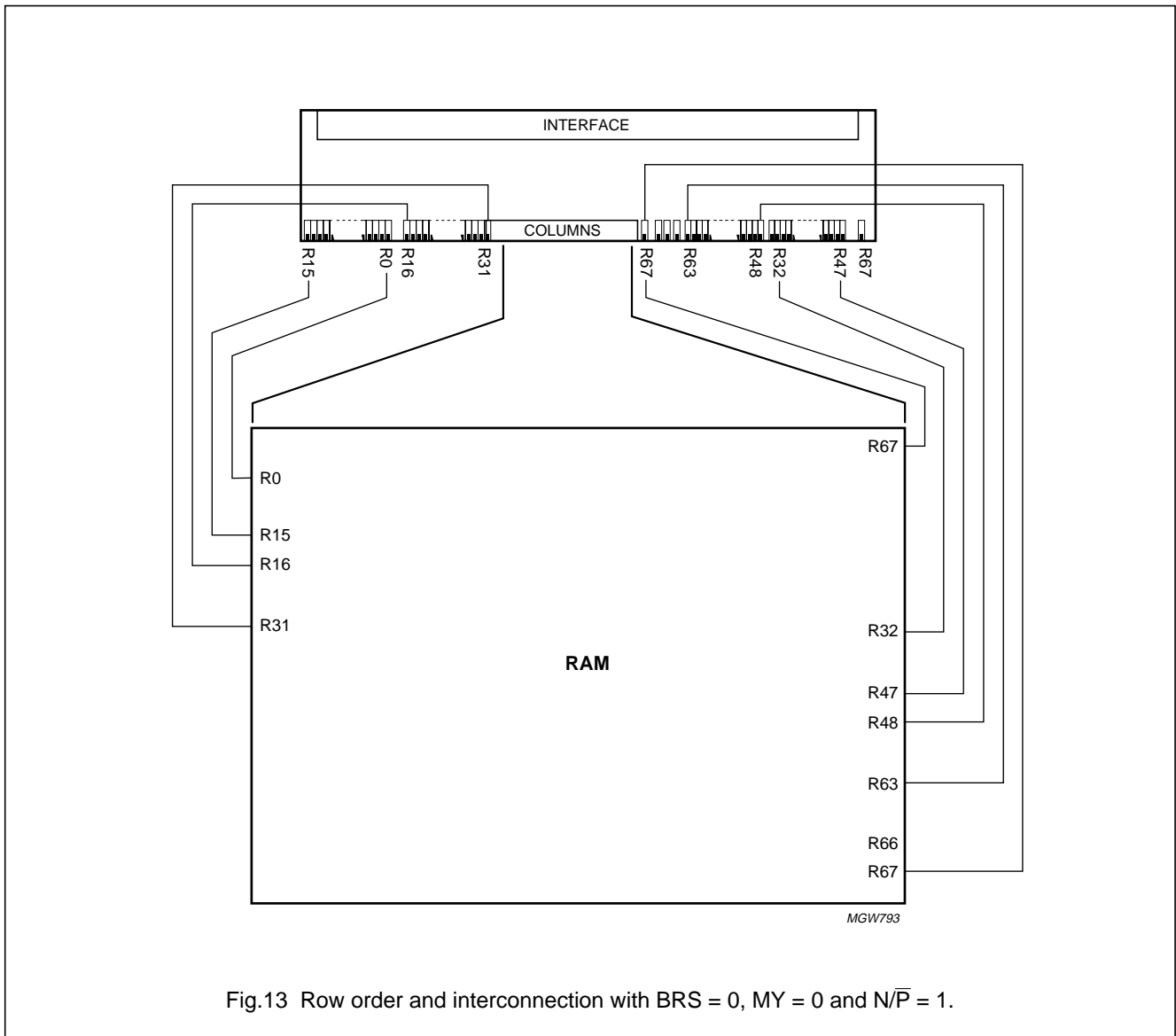


Fig.13 Row order and interconnection with BRS = 0, MY = 0 and N/P = 1.

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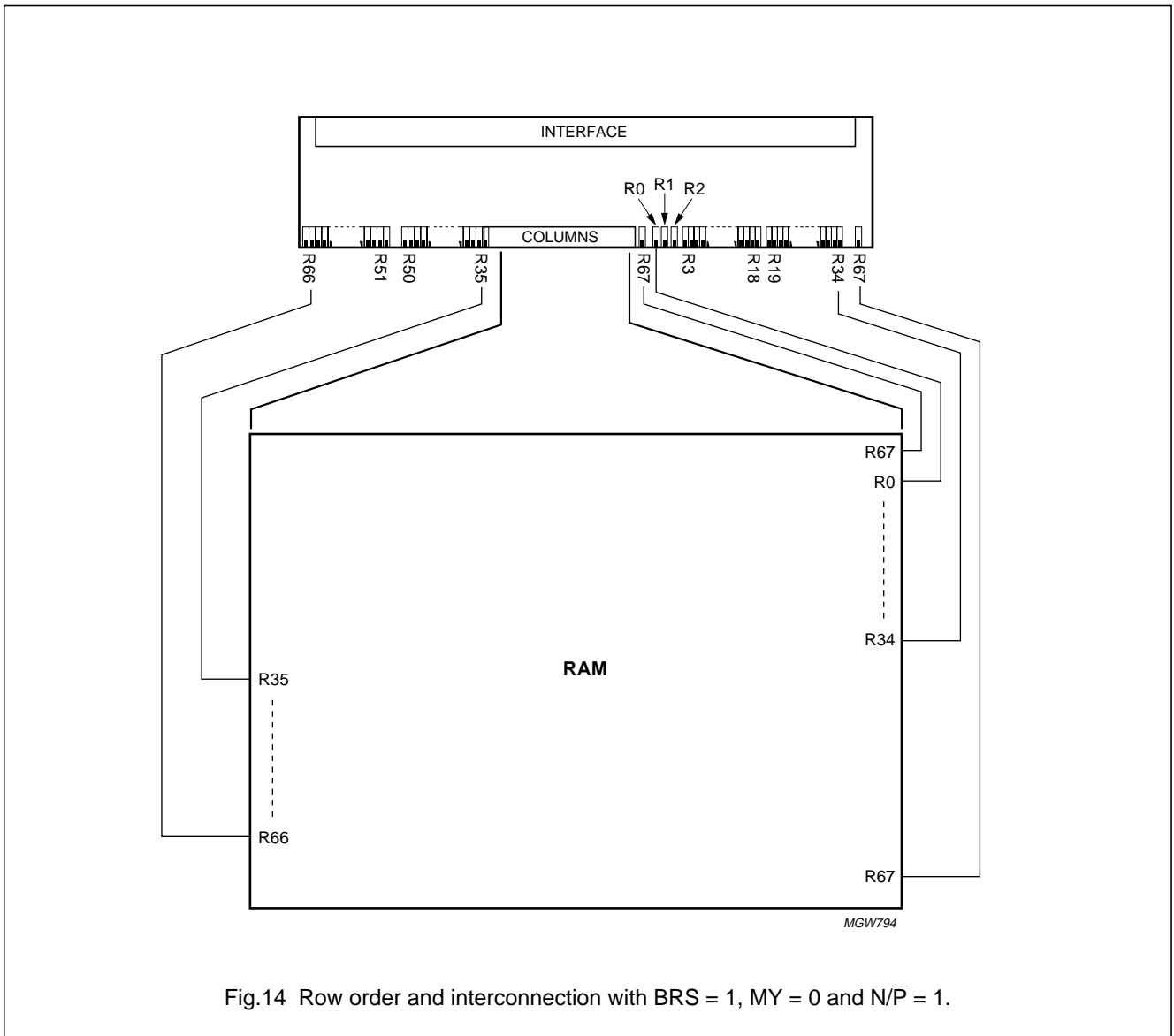


Fig.14 Row order and interconnection with BRS = 1, MY = 0 and $N/\bar{P} = 1$.

(67 + 1) × 102 pixels matrix LCD driver**PCF8813****8 PARALLEL INTERFACES**

The parallel interface is an 8-bit bidirectional interface for communication between the microcontroller and the LCD driver chip. Two different parallel interfaces can be selected by the inputs PS2, PS1 and PS0.

8.1 6800-type parallel interface

The interface functions of the 6800-type parallel interface are shown in Table 2.

Table 2 6800-type parallel interface function

| D/C | R/W \bar{R} | OPERATION |
|-----|---------------|----------------------|
| 0 | 0 | command data write |
| 0 | 1 | read status register |
| 1 | 0 | display data write |
| 1 | 1 | none |

The 6800-type parallel interface can be configured to have the clock connected to the Enable input (E) with timing as shown in Fig.38, or with the clock connected to the chip select input (\overline{SCE}) and the Enable (E) is tied HIGH with timing as shown in Fig.39. The PCF8813 is capable of detecting these different modes automatically.

8.2 8080-type parallel interface

Table 3 shows the interface functions of the 8080-type parallel interface.

Table 3 6800-type parallel interface function

| D/C | \overline{RD} | \overline{WR} | OPERATION |
|-----|-----------------|-----------------|----------------------|
| 0 | 1 | 0 | command data write |
| 0 | 0 | 1 | read status register |
| 1 | 1 | 0 | display data write |
| 1 | 1 | 1 | none |

9 SERIAL INTERFACES

Communication with the microcontroller can also be via a clock-synchronized serial peripheral interface. It is possible to select two different 3-line interfaces (SPI and serial interface) or a 4-line serial interface (SPI). Selection of the interface is made with the inputs PS2, PS1 and PS0 (see Section 7.1).

9.1 Serial peripheral interface

The Serial Peripheral Interface (SPI) is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver. The 3-line interface requires a chip enable input (\overline{SCE}), serial clock (SCLK) and serial data (SDATA). For the 4-line serial interface, a separate D/C line is added. The PCF8813 is connected to the serial data I/O (SDATA) of the microcontroller via the pads data input (SDATA) and data output (SDOUT) connected together.

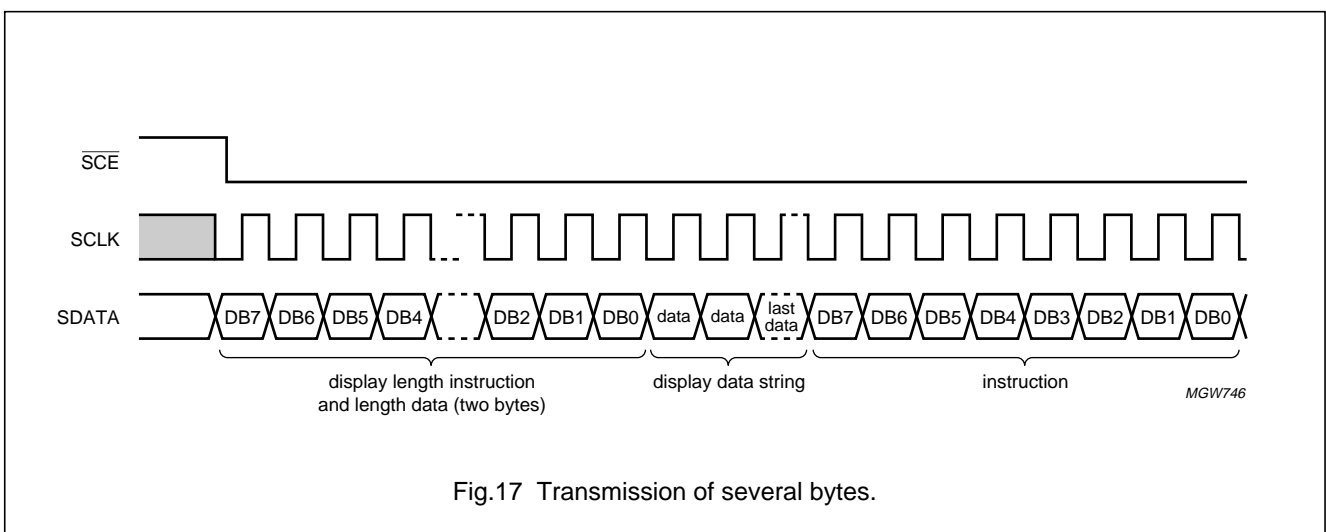
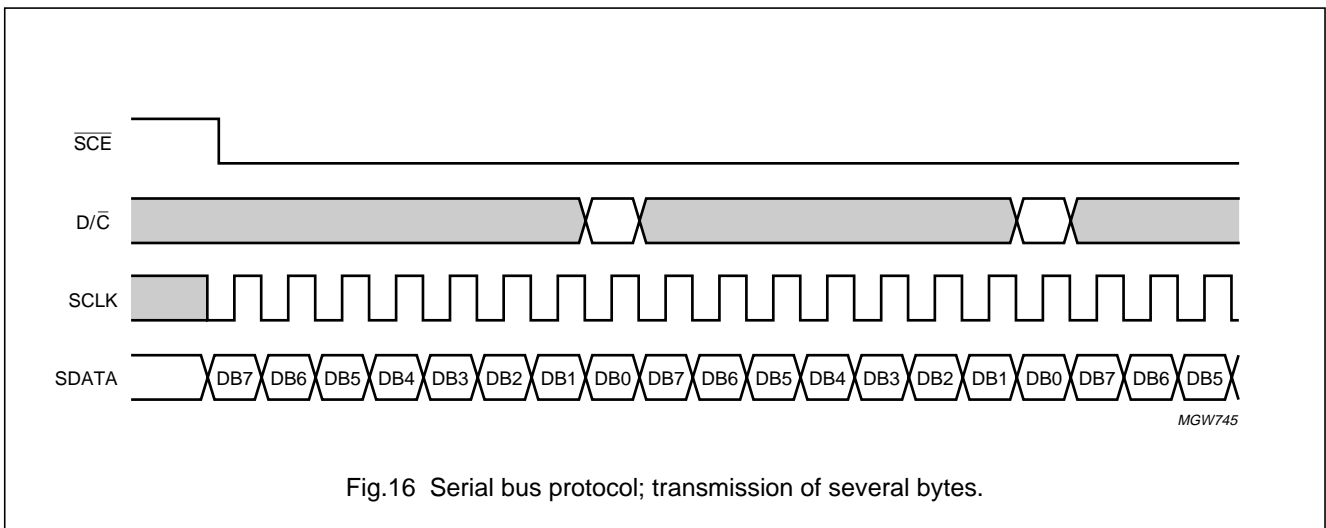
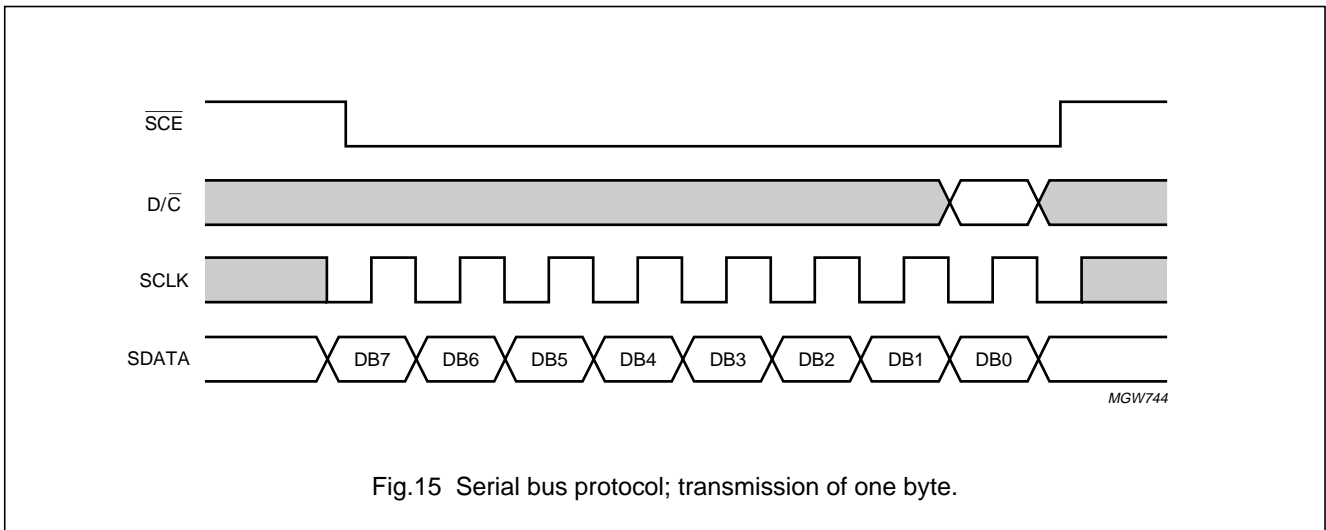
9.1.1 WRITE MODE

The display data/command indication may be controlled via software or by the D/C select input. When the D/C input is used, display data is transmitted when D/C is HIGH, and command data is transmitted when D/C is LOW (see Figs 15 and 16). When D/C is not used, the display data length instruction is used to indicate that a specific number of display data bytes (1 to 256) are to be transmitted (see Fig.17). The byte that follows the display data string is handled as an instruction command.

If \overline{SCE} is pulled HIGH during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data is valid. The next byte received will be handled as an instruction command (see Fig.18).

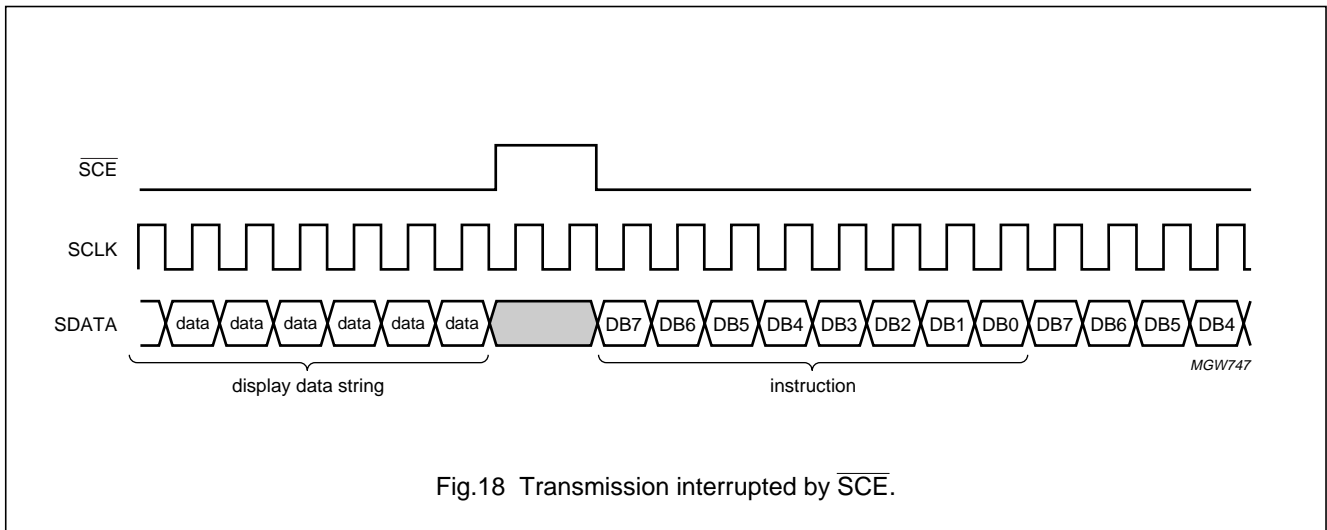
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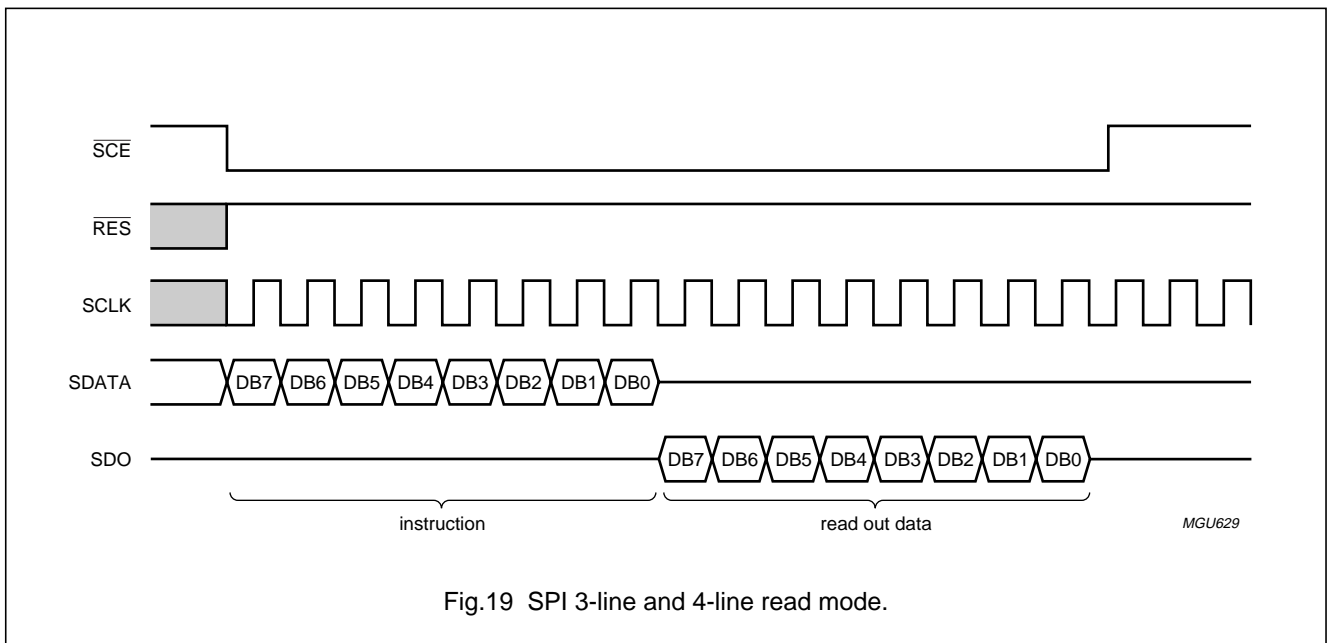


9.1.2 READ MODE

The interface read mode means that the microcontroller reads data from the PCF8813. To do so the microcontroller first has to send a command, the read status command, and then the PCF8813 will respond by transmitting data on the SDO line. After that SCE is required to go HIGH before a new command is sent (see Fig.17).

The PCF8813 samples SDATA at rising SCLK edges, but shifts SDO data at falling SCLK edges. Thus the microcontroller reads SDO data at rising SCLK edges.

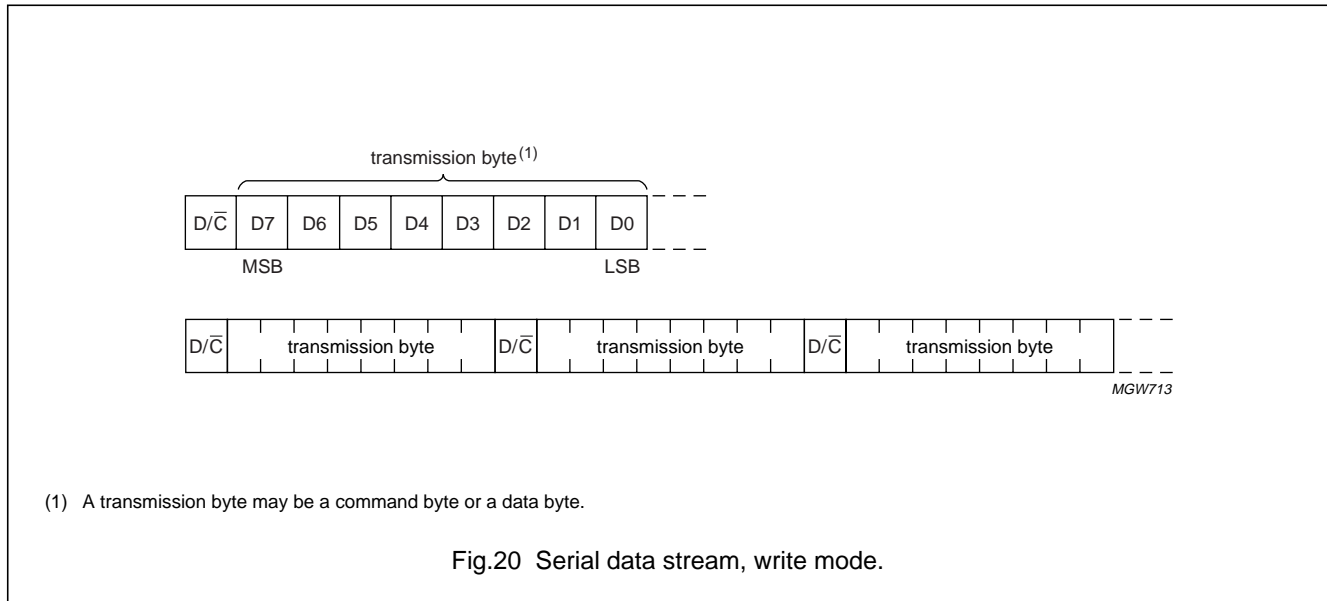
After the read status command has been sent, the SDATA line must be set to 3-state not later than at the falling SCLK edge of the last bit (see Fig.19).



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9.2 Serial interface (3-line)



The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The three lines are: \overline{SCE} (chip enable), SCLK (serial clock) and SDATA (serial data). The PCF8813 is connected to the SDA of the microcontroller by the SDATA (data input) and SDO (data output) pads which are connected together.

9.2.1 WRITE MODE

In the write mode of the interface, the microcontroller writes commands and data to the PCF8813. Each data packet contains a control bit D/\overline{C} and a transmission byte. If D/\overline{C} is LOW, the following byte is interpreted as a command byte. If D/\overline{C} is HIGH, the following byte is stored in the display data RAM. The address counter is incremented automatically after every data byte. Figure 20 shows the general format of the write mode and the definition of the transmission byte.

Any instruction can be sent in any order to the PCF8813. The MSB of a byte is transmitted first. The serial interface is initialized when \overline{SCE} is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on \overline{SCE} enables the serial interface and indicates the start of data transmission.

Figures 21, 22 and 23 show the protocol of the write mode:

- When \overline{SCE} is HIGH, SCLK clocks are ignored; the serial interface is initialized during the HIGH time of \overline{SCE} (see Fig.21)
- At the falling \overline{SCE} edge SCLK must be LOW (see Fig.41)
- SDATA is sampled at the rising edge of SCLK
- D/\overline{C} indicates whether the byte is a command ($D/\overline{C} = 0$) or RAM data ($D/\overline{C} = 1$); it is sampled with the first rising SCLK edge
- If \overline{SCE} stays LOW after the last bit of a command/data byte, the serial interface is ready for the D/\overline{C} -bit of the next byte at the next rising edge of SCLK (see Fig.22).
- A reset pulse with \overline{RES} interrupts the transmission and the data being written into the RAM may be corrupted. The registers are cleared. If \overline{SCE} is LOW after the rising edge of \overline{RES} , the serial interface is ready to receive the D/\overline{C} -bit of a command/data byte (see Fig.23).

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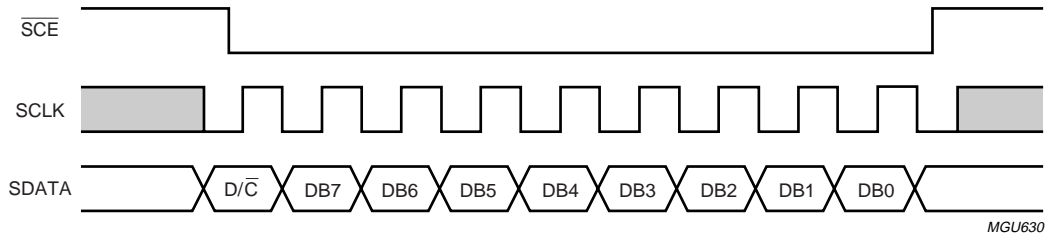


Fig.21 Serial interface (3-line), write mode - control bit followed by a transmission byte.

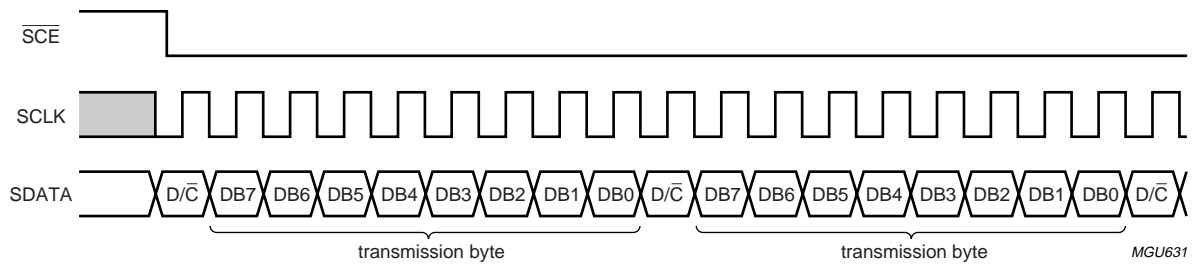


Fig.22 Serial interface (3-line), write mode - transmission of several bytes.

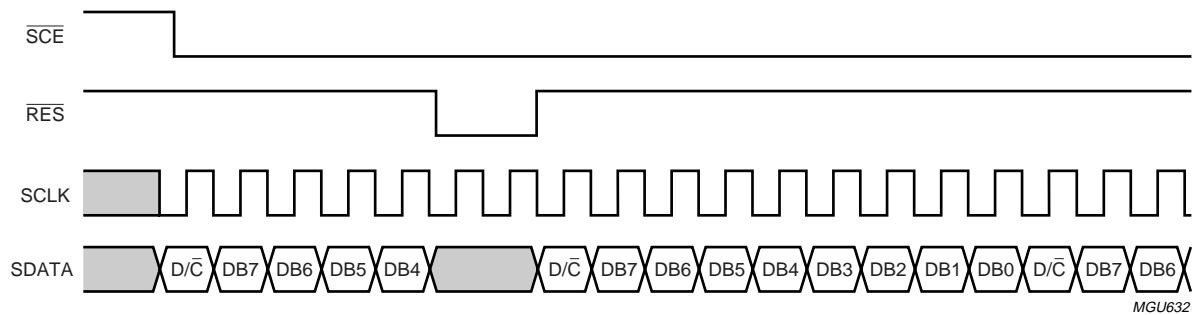


Fig.23 Serial interface (3-line), write mode - interrupted by reset (\overline{RES}).

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9.2.2 READ MODE

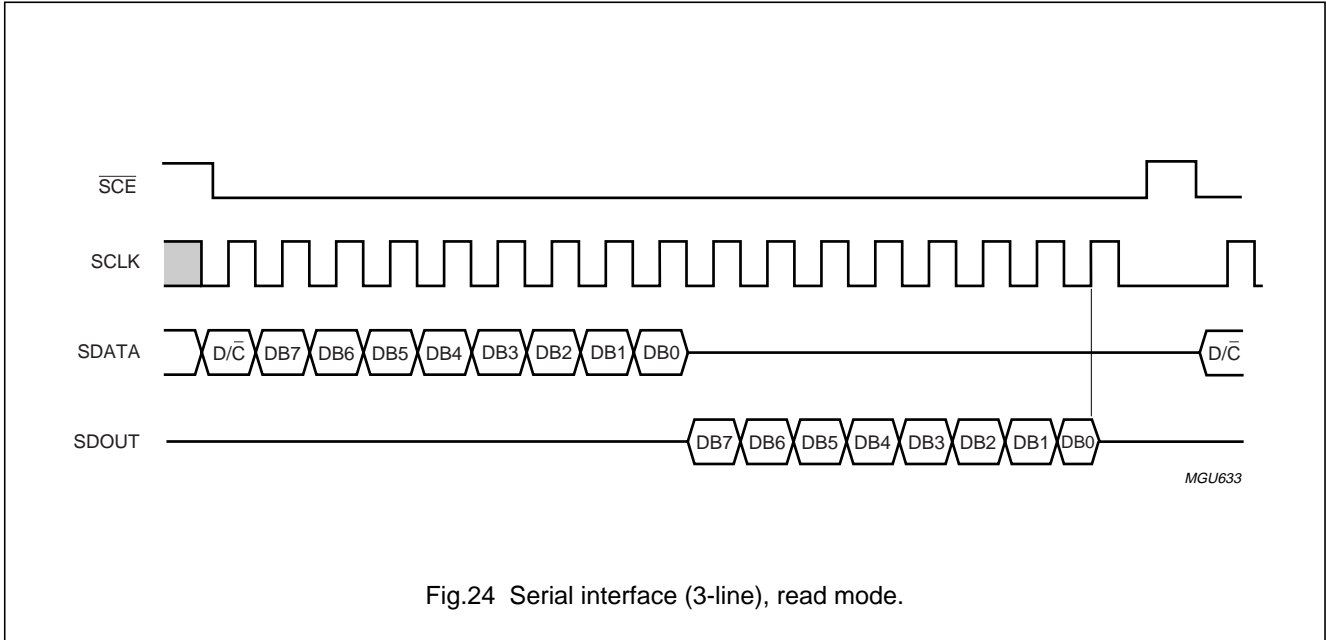


Fig.24 Serial interface (3-line), read mode.

In the read mode of the interface, that the microcontroller reads data from the PCF8813. To do this the microcontroller has first to send a command, then the read status command, and then the PCF8813 will respond by transmitting data on the SDOUT line. After that, \overline{SCE} is required to go HIGH before a new command is sent (see Fig.24).

The PCF8813 samples the SDATA data at rising SCLK edges, but shifts SDOUT data at falling SCLK edges. Thus the microcontroller reads SDOUT data at rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state not later than at the falling SCLK edge of the last bit.

The 8th read bit is shorter than the others because it is terminated by the rising SCLK edge (see Fig.24). The last rising SCLK edge sets SDOUT to 3-state after a delay time (see time t_4 in Fig.44).

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10 I²C-BUS INTERFACE (Hs-MODE)

10.1 Characteristics of the I²C-bus (Hs-mode)

The I²C-bus Hs-mode is for bidirectional, two-line communication between different ICs or modules with speeds up to 3.4 MHz. The only difference between Hs-mode slave devices and Fast-mode slave devices is the speed at which they operate, therefore the buffers on the SLCH and SDAH outputs⁽¹⁾ have an open-drain. This is the same for I²C-bus master devices which have an open-drain SDAH output and a combination of open-drain pull-down and current source pull-up circuits on the SCLH output. Only the current source of one master is enabled at any one time, and only during Hs-mode. Both lines must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

(1) In Hs-mode, SCL and SDA lines operating at the higher frequency are referred to as SCLH and SDAH.

10.1.1 SYSTEM CONFIGURATION

- Transmitter: the device that sends the data to the bus
- Receiver: the device that receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: procedure to synchronize the clock signals of two or more devices.

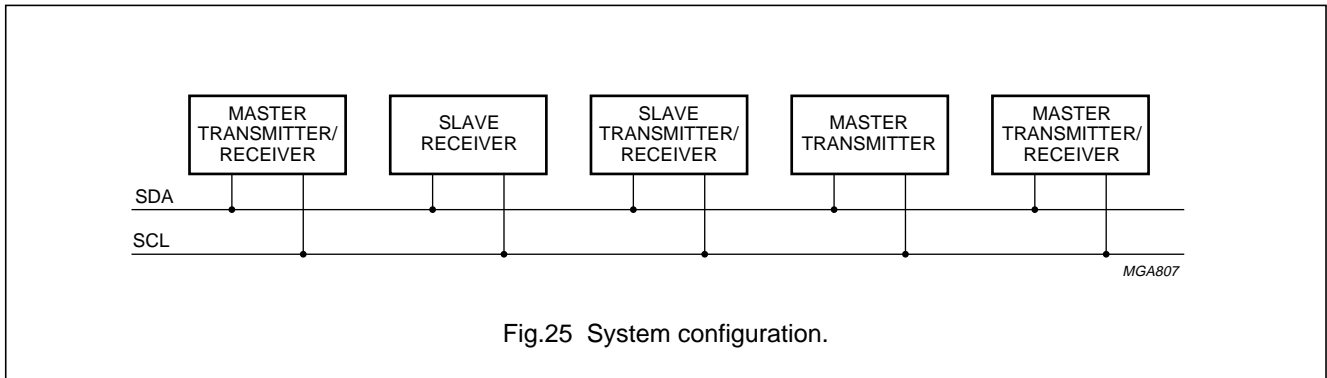


Fig.25 System configuration.

10.1.2 BIT TRANSFER

One data bit is transferred during each clock pulse (see Fig.26). The data on the SDAH line must remain stable

during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

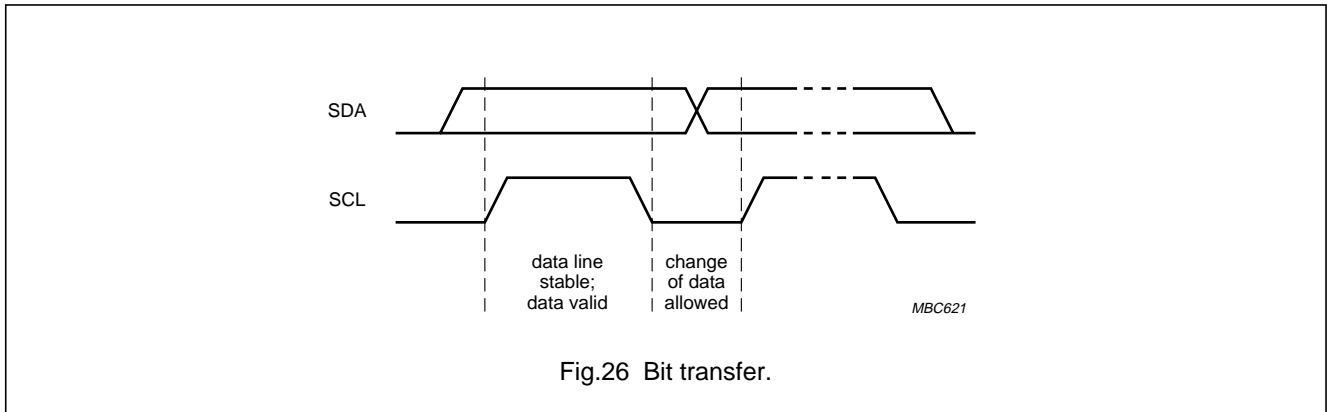


Fig.26 Bit transfer.

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10.1.3 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy (see Fig.27). A HIGH-to-LOW transition of the data

line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

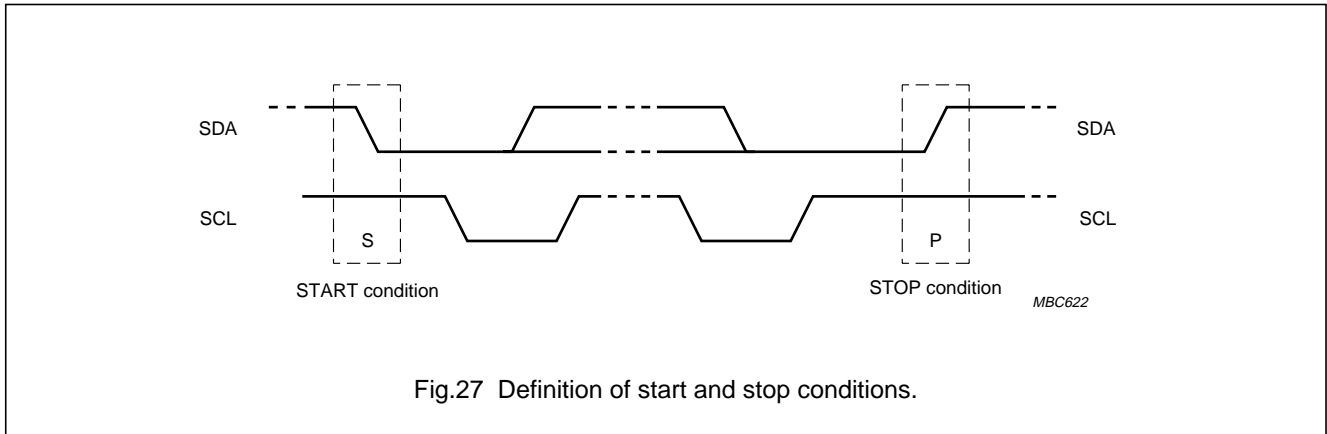


Fig.27 Definition of start and stop conditions.

10.1.4 ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit (see Fig.28). The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the

slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

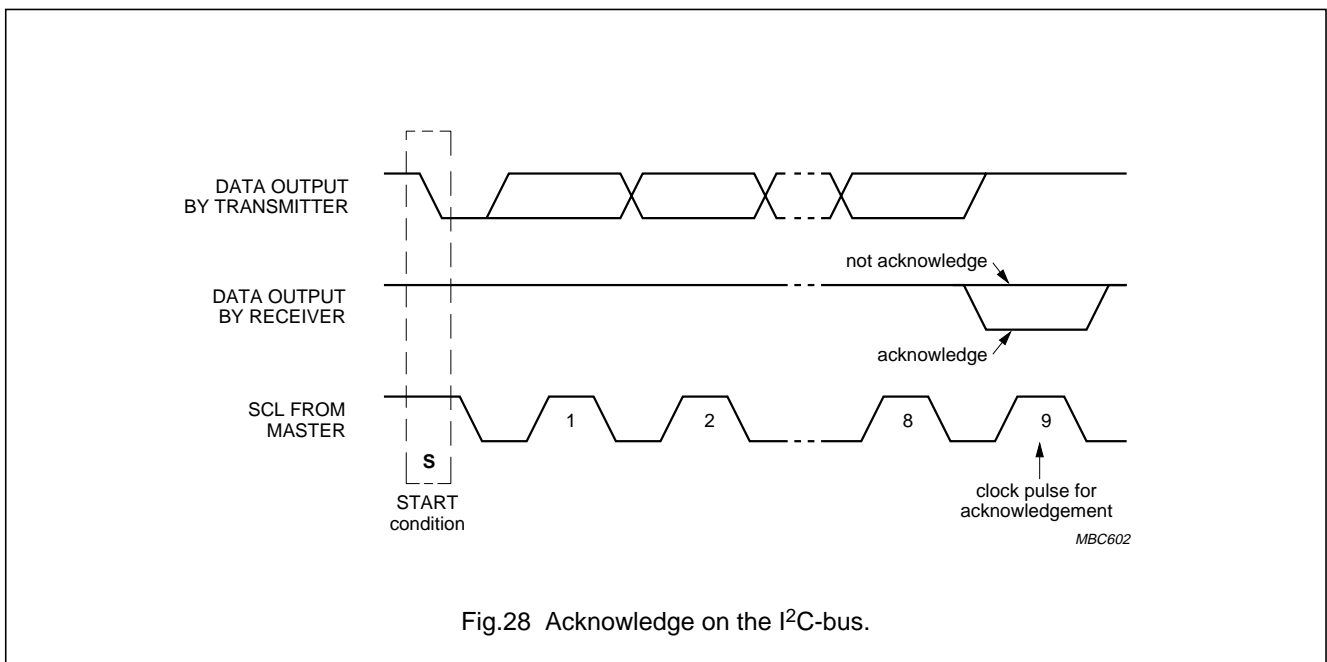


Fig.28 Acknowledge on the I²C-bus.

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10.2 I²C-bus Hs-mode protocol

The PCF8813 is a slave receiver/transmitter. If data is to be read from the device the SDAH pad must be connected, otherwise SDAHOUT may be unused.

Hs-mode can only commence after the following conditions:

- START condition (S)
- 8-bit master code (00001XXX)
- Not-acknowledge bit (\bar{A}).

The master code has two functions, as shown in Figs 29 and 30, it allows arbitration and synchronization between competing masters at Fast-mode speeds, resulting in one winner. Also the master code indicates the beginning of an Hs-mode transfer.

As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge (\bar{A}). After this \bar{A} -bit, and the SCLH line has been pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_{H} the current-source pull-up circuit for the SCLH signal (see Fig.30).

The active master will then send a repeated START condition (Sr) followed by a 7-bit slave address with a R/\bar{W} -bit, and receives an acknowledge bit (A) from the

selected slave. After each acknowledge bit (A) or not-acknowledge bit (\bar{A}) the active master disables its current-source pull-up circuit. The active master re-enables its current source again when all devices have released and the SCLH signal reaches a HIGH level. The rising of the SCLH is done by a resistor pull-up and so slower, the last part of the SCLH rise time is speeded up because the current-source is enabled. Data transfer only switches back to Fast-mode after a STOP condition (P).

A write sequence after the Hs-mode is selected is given in Fig.29. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After acknowledgement of a write (W) cycle, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines CO and D/ \bar{C} , plus a data byte (see Fig.31 and Table 4).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. The control and data bytes are also acknowledged by all addressed slaves on the bus.

Table 4 CO and D/ \bar{C} definition

| BIT | 0/1 | R/W | ACTION |
|--------------|-----|-----|---|
| CO | 0 | N/A | last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition |
| | 1 | | another control byte will follow the data byte unless a STOP or RE-START condition is received |
| D/ \bar{C} | 0 | 0 | data byte will be decoded and used to set-up the device |
| | | 1 | data byte will return the status byte |
| | 1 | 0 | data byte will be stored in the display RAM |
| | | 1 | RAM read back is not supported |

After the last control byte, depending on the D/ \bar{C} bit setting, a series of display data bytes or command data bytes may follow. If the D/ \bar{C} -bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is updated automatically and the data is directed to the intended PCF8813. If the D/ \bar{C} -bit of the last control byte was set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8813. At the end of the transmission the I²C-bus master issues a STOP

condition (P) and switches back to Fast-mode, however, to reduce the overhead of the master code, its possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

A read sequence (see Fig.32) follows after the Hs-mode is selected. The PCF8813 will immediately start to output the requested data until a NOT acknowledge is transmitted by the master. Before the read access, the user has to set the D/ \bar{C} -bit to the appropriate value by a preceding write access. The write access should be terminated by a RE-START condition so that the HS-mode is not disabled.

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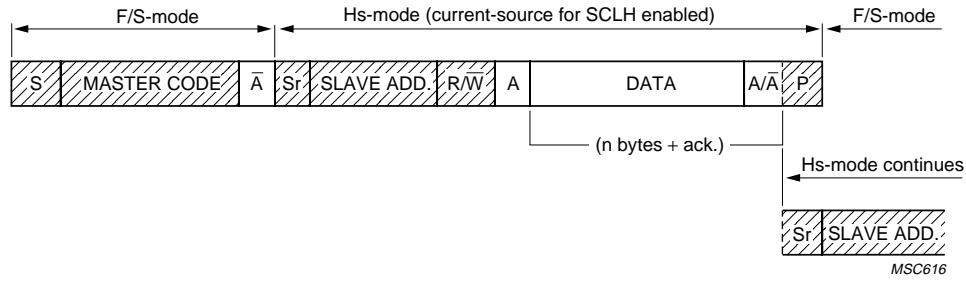


Fig.29 Data transfer format in Hs-mode.

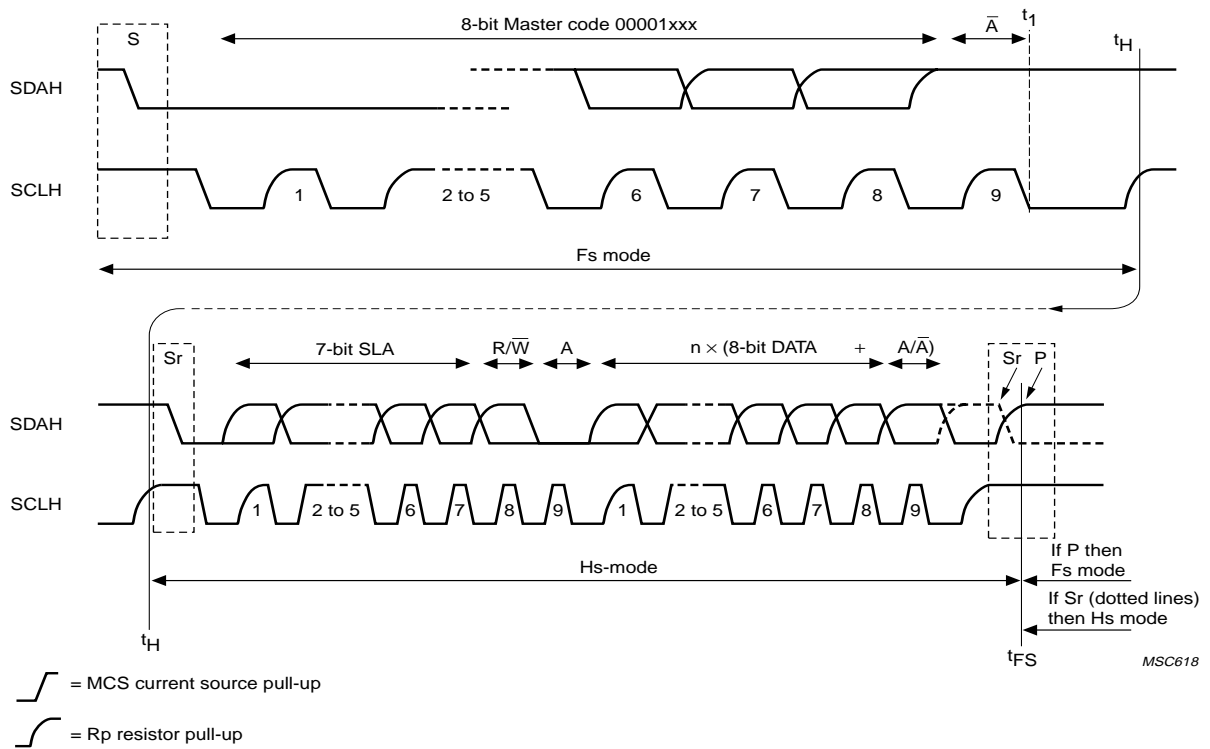


Fig.30 Complete data transfer in Hs-mode.

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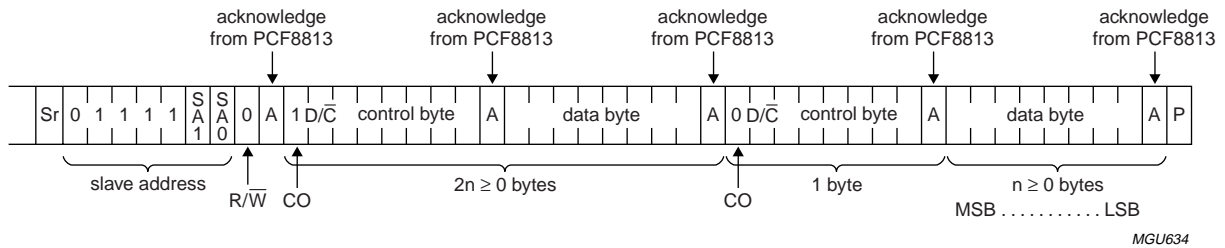


Fig.31 Master transmits in Hs-mode to slave receiver; write mode.

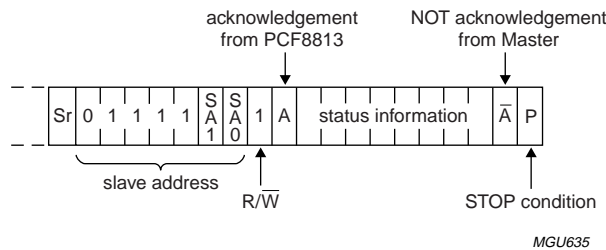


Fig.32 Master receives from slave transmitter (status register is read); read mode.

10.3 Command decoder

The command decoder identifies command words that arrive on the I²C-bus.

- Pairs of bytes
 - first byte determines whether information is display or instruction data
 - second byte contains information.
- Stream of information bytes after CO = 0; display or instruction data depending on last D/C-bar-bit.

The most significant bit of a control byte is the continuation bit CO. If this bit is logic 1, it indicates that only one data byte, either command or RAM data, will follow. If the bit is logic 0, it indicates that a series of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM data/command bit D/C-bar. When this bit is logic 1, it indicates that a RAM data byte will be transferred next. If the bit is at logic 0, it indicates that a command byte will be transferred next.

(67 + 1) × 102 pixels matrix LCD driver**PCF8813****11 INSTRUCTIONS**

The PCF8813 interfaces via the 8-bit parallel interface, two different 3-line serial interfaces, 4-wire serial interface or an I²C-bus interface. Processing of the instructions does not require the display clock.

In the case of the parallel and 4-wire serial interface, data accesses to the PCF8813 can be divided into two areas; those that define the operating mode of the device, and those that fill the display RAM; the distinction being the D/C input. When the D/C input is set to logic 0, the chip will respond to instructions as defined in Table 5. When the D/C bit is at logic 1, the chip will send data into the RAM.

When the 3-wire serial interface or the I²C-bus interface is used, the distinction between instructions that define the

operating mode of the device and those that fill the display RAM is made respectively by the display data length instruction (4-line SPI) or by D/C bit in the data stream (3-line serial interface and I²C-bus interface).

There are four types of instructions:

- Defining PCF8813 functions such as display configuration, etc.
- Setting internal RAM addresses
- Performing data transfer with internal RAM
- Other instructions.

In normal use, category 3 instructions are used most frequently. To lessen the MPU program load, automatic incrementing by one of the internal RAM address pointers after each data write is implemented.

Table 5 Instruction set

Instructions not expressly defined in this table and reserved instructions are not allowed in PCF8813 applications.

| INSTRUCTION | D/C | R/W | COMMAND BYTE | | | | | | | | DESCRIPTION |
|--------------------------------|-----|-----|--------------|-----|-----|-----|-----|-----|------------------|------------------|---|
| | | | DB7 (MSB) | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 (LSB) | |
| H = 0 or 1 | | | | | | | | | | | |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | no operation |
| Function set | 0 | 0 | 0 | 0 | 1 | MX | MY | PD | V | H | Power-down control; entry mode |
| Read status byte | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | δ ⁽¹⁾ | δ ⁽¹⁾ | read status byte for serial and I ² C-bus interfaces |
| Read status byte | 0 | 1 | BUSY | DON | RES | MF2 | MF1 | MF0 | DS1 | DS0 | reads parallel interface status byte |
| Write data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | writes data to RAM |
| H = 0 | | | | | | | | | | | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | do not use |
| Display control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | 0 | E | sets display configuration |
| Set lower/higher program range | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | PRS | V _{LCD} programming range |
| Set power control HVgen on/off | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | PC | switch HVgen on/off |
| Display configuration | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | δ ⁽¹⁾ | double command byte: set data order; top/bottom row swap mode |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0 | 0 | BRS | |

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| INSTRUCTION | D/C | R/W | COMMAND BYTE | | | | | | | | DESCRIPTION |
|--------------------------------------|-----|-----|--------------|------------|------------|------------|----------------|----------------|----------------|----------------|--|
| | | | DB7 (MSB) | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 (LSB) | |
| Set display data length | 0 | 0 | 0 | 1 | 1 | 1 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte; set display data length, only used in 3-line SPI |
| | 0 | 0 | 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Set Y address of RAM | 0 | 0 | 0 | 1 | 0 | 0 | Y_3 | Y_2 | Y_1 | Y_0 | sets Y address of RAM: $0 \leq Y \leq 9$ |
| Set maximum Y address | 0 | 0 | 0 | 1 | 0 | 1 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: set maximum Y: $0 \leq Y \leq 8$ |
| | 0 | 0 | 0 | 0 | 0 | 0 | Y_{max3} | Y_{max2} | Y_{max1} | Y_{max0} | |
| Set maximum X address | 0 | 0 | 0 | 1 | 1 | 0 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: set maximum X: $0 \leq X \leq 101$ |
| | 0 | 0 | 0 | X_{max6} | X_{max5} | X_{max4} | X_{max3} | X_{max2} | X_{max1} | X_{max0} | |
| Set X address of RAM | 0 | 0 | 1 | X_6 | X_5 | X_4 | X_3 | X_2 | X_1 | X_0 | sets X address of RAM: $0 \leq X \leq 101$ |
| H = 1 | | | | | | | | | | | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | |
| Temperature compensation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | TC_1 | TC_0 | set temperature coefficient (TCx) |
| Set HVgen stages | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S_1 | S_0 | set multiplication factor |
| Bias system | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BS_2 | BS_1 | BS_0 | set bias system (BSx) |
| Reserved | 0 | 0 | 0 | 1 | 1 | 0 | 0 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: do not use |
| | 0 | 0 | 0 | 0 | 0 | 0 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | |
| Normal or partial display mode | 0 | 0 | 0 | 1 | 0 | 1 | 0 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: set normal or partial display mode |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | N/\bar{P} | |
| Free programmable MUX rate | 0 | 0 | 0 | 1 | 1 | 0 | 1 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: set mask register for FPMR mode (1 : 9, 17, and 25 to 64) |
| | 0 | 0 | M_7 | M_6 | M_5 | M_4 | M_3 | M_2 | M_1 | M_0 | |
| Set initial row to be displayed | 0 | 0 | 0 | 1 | 0 | 0 | 1 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte: set start row $0 \leq X \leq 66$ |
| | 0 | 0 | 0 | C_6 | C_5 | C_4 | C_3 | C_2 | C_1 | C_0 | |
| Set RAM line address for initial row | 0 | 0 | 0 | 1 | 0 | 1 | 1 | $\delta^{(1)}$ | $\delta^{(1)}$ | $\delta^{(1)}$ | double command byte; sets RAM line address to be displayed $0 \leq L \leq 66$ |
| | 0 | 0 | 0 | L_6 | L_5 | L_4 | L_3 | L_2 | L_1 | L_0 | |

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| INSTRUCTION | D/C | R/W | COMMAND BYTE | | | | | | | | DESCRIPTION |
|-------------------------------------|-----|-----|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------------------------|
| | | | DB7 (MSB) | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 (LSB) | |
| Disable OTP circuitry | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | disable OTP circuitry |
| Enter module maker calibration mode | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | module maker calibration |
| Software reset | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | enable software reset |
| Set V_{PR} | 0 | 0 | 1 | V_{PR6} | V_{PR5} | V_{PR4} | V_{PR3} | V_{PR2} | V_{PR1} | V_{PR0} | write V_{PR} to register |

Note

1. δ = don't care.

Table 6 Explanation of mnemonics used in Table 5

| BIT | 0 | 1 | RESET STATE |
|----------------|--|----------------------------------|-------------|
| PD | chip active | chip is in Power-down mode | 1 |
| H | basic command set | extended command set | 0 |
| V | horizontal addressing | vertical addressing | 0 |
| PC | power control off | power control on | 1 |
| MX | normal X addressing | X address is mirrored | 0 |
| MY | display is not vertically mirrored | display is vertically mirrored | 0 |
| TRS | top rows are not mirrored | top rows are mirrored | 0 |
| BRS | bottom rows are not mirrored | bottom rows are mirrored | 0 |
| DO | LSB is on top | MSB is on top | 1 |
| PRS | V_{LCD} programming range LOW | V_{LCD} programming range HIGH | 0 |
| N/P | partial display driving mode | normal display driving mode | 1 |
| C[6:0] | sets the initial R0 of the display.; this command cannot access R67 (icon row) | | 0000000 |
| L[6:0] | sets the line address of the display RAM to be displayed on the initial R0; this command cannot access R67 | | 0000000 |
| $Y_{max}[3:0]$ | sets maximum Y address for wraparound | | 1000 |
| $X_{max}[6:0]$ | sets the maximum X address | | 1100101 |
| D, E | display control; see Table 8 | | 00 |
| TC[1:0] | set temperature coefficient; see Table 9 | | 00 |
| S[1:0] | set voltage multiplication factor; see Table 10 | | 00 |
| BS[2:0] | bias system | | 000 |
| $V_{PR}[6:0]$ | V_{LCD} programming | | 0000000 |
| M[7:0] | set partial display (full display = 11111111) | | 11111111 |

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Table 7 Read status byte

| BIT | FUNCTION |
|-------------------------|--|
| BUSY | 0 = chip is able to accept new commands; 1 = chip is unable to accept new commands |
| DON | 0 = display OFF; 1 = display ON |
| $\overline{\text{RES}}$ | 0 = reset NOT in progress; 1 = reset in progress |
| MF[2:0] | manufacturer identification bits |
| DS[1:0] | device recognition; currently has a fixed value of 00 (recognition bits for a driver with 64 to 67 rows) |

Table 8 Display control; bits D and E

| D | E | FUNCTION |
|---|---|-------------------------|
| 0 | 0 | display blank |
| 1 | 0 | normal mode |
| 0 | 1 | all display segments on |
| 1 | 1 | inverse video mode |

Table 9 Set temperature coefficient; bits TC[1:0]

| TC ₁ | TC ₀ | FUNCTION |
|-----------------|-----------------|--|
| 0 | 0 | V _{LCD} temperature coefficient 0 |
| 0 | 1 | V _{LCD} temperature coefficient 1 |
| 1 | 0 | V _{LCD} temperature coefficient 2 |
| 1 | 1 | V _{LCD} temperature coefficient 3 |

Table 10 Set voltage multiplication factor; bits S[1:0]

| S ₁ | S ₀ | FUNCTION |
|----------------|----------------|------------------------|
| 0 | 0 | 2 × voltage multiplier |
| 0 | 1 | 3 × voltage multiplier |
| 1 | 0 | 4 × voltage multiplier |
| 1 | 1 | 5 × voltage multiplier |

11.1 Initialization

Immediately following Power-on, all internal registers as well as the RAM content are undefined. A $\overline{\text{RES}}$ pulse **must** be applied to the reset input.

Reset is accomplished by applying an external reset pulse (active LOW) at the pad RES. When reset occurs within the specified time all internal registers are reset, however the RAM is still undefined. The $\overline{\text{RES}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches $V_{DD(\text{min})}$ (or higher) within a maximum time t_{VHRL} after V_{DD} going HIGH (see Fig.37).

A reset can also be made by sending a reset command. This command can be used during normal operating but not to initialize the chip after Power-on.

11.2 Reset function

After reset the LCD driver has the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Display blank (D and E = 00)
- Address counter X[6:0] = 0000000 and Y[3:0] = 0000
- Temperature control mode TC[1:0] = 00
- V_{LCD} is equal to 0 and PRS = 0
- Power control is enabled (PC = 1)
- Normal row driving of display (N/ $\overline{\text{P}}$ = 1)
- Partial mode set for all rows available (M[7:0] = 11111111)
- HV generator programmed off (V_{PR}[6:0] = 0000000)
- 2 × voltage multiplier (S[1:0] = 00)
- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- Data order DO = 0
- All LCD outputs at V_{SS} (display off)
- Bias system (BS[2:0] = 000)
- Display start line set to R0 (C[6:0] = 000000)
- RAM line address set to 0 (L[6:0] = 000000)
- Maximum X address = 101 (X_{max}[6:0] = 1100101)
- Maximum Y address = 8 (Y_{max}[3:0] = 1000)
- Display is not mirrored (MX = 0; MY = 0 and BRS = 0).

11.3 Power-down mode

Power-down mode gives the following circuit status:

- V_{LCD} discharges to V_{SS} as Power-down mode occurs
- All LCD outputs go to V_{SS} (display off)
- Bias generator and V_{LCD} generator switch-off, V_{LCD} can be disconnected
- Oscillator switches off (external clock is possible)
- RAM contents are not cleared; RAM data can be written.

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Bits D and E (see Table 8) select the display mode.

When bit MX = 0, the display RAM is written from left to right (X = 0 is on the left side and X = 101 is on the right side of the display). When bit MX = 1, the display RAM is written from right to left (X = 0 is on the right side and X = 101 is on the left side of the display).

The bit MX has an impact on the way the RAM is written. So if horizontal mirroring of the display is required, the RAM must first be rewritten.

When bit MY = 1, the display is mirrored vertically. A change of bit MY has an immediate effect on the display.

When bit V = 0, horizontal addressing is selected and data is written into the DDRAM as shown in Fig.5. When bit V = 1, vertical addressing is selected, then data is written into the DDRAM as shown in Fig.6.

11.5 Set Y address of RAM

Bits Y[3:0] define the Y address vector address of the display RAM.

Table 11 Range of Y address and allowable X range

| Y ADDRESS | | | | RAM CONTENT | ALLOWED X RANGE |
|-----------|---|---|---|-----------------------|-----------------|
| 3 | 2 | 1 | 0 | | |
| 0 | 0 | 0 | 0 | bank 0 (display RAM) | 0 to 101 |
| 0 | 0 | 0 | 1 | bank 1 (display RAM) | 0 to 101 |
| 0 | 0 | 1 | 0 | bank 2 (display RAM) | 0 to 101 |
| 0 | 0 | 1 | 1 | bank 3 (display RAM) | 0 to 101 |
| 0 | 1 | 0 | 0 | bank 4 (display RAM) | 0 to 101 |
| 0 | 1 | 0 | 1 | bank 5 (display RAM) | 0 to 101 |
| 0 | 1 | 1 | 0 | bank 6 (display RAM) | 0 to 101 |
| 0 | 1 | 1 | 1 | bank 7 (display RAM) | 0 to 101 |
| 1 | 0 | 0 | 0 | bank 8 (display RAM) | 0 to 101 |
| 1 | 0 | 1 | 0 | bank 10 (display RAM) | 0 to 101 |

In bank 8 only three bits are accessed, and in bank 10 only one bit is accessed.

11.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 101 (65H).

11.7 Set maximum X address or Y address

These two commands ($X_{max}[6:0]$ and $Y_{max}[3:0]$) set the maximum address for wraparound to occur for the columns. The range of X_{max} is 0 to 101. The maximum Y address also sets the Y address for wraparound to occur. The range of Y_{max} is 0 to 8. By design, the maximum Y setting cannot access bank 10. X_{max} and Y_{max} together also define when wraparound-to-zero takes place. These two commands are effective only when writing to the RAM.

11.8 Set display start line, initial start row and row 0

Set display start line L[6:0] allows the display line address of the display RAM to be chosen. The range is from line 0 to line 66 inclusive. The RAM address line 67 is not available for this command as it is reserved for icons. This command has an effect on the mapping between the data of the RAM and the display. The L address specifies which rows of the RAM are output to which row outputs of the display. The value of the L address defines which row of the RAM will be row 0. Row 0 of the display can in turn be set by the set initial row command C[6:0].

Figure 33 shows an example of how RAM data is mapped onto the display. In this example, the L command sets the data on line 8 of the RAM to be displayed. This data is displayed on a row set by the C command (16). When L and C are set to 8 and 16 respectively, data from RAM lines 4 to 7 is displayed on display rows 12 to 15 and RAM data from lines 15 to 18 is displayed on display lines 23 to 26.

When MY is active (MY = 1), the data from Fig.33 is mapped from the RAM to the display as shown in Fig.34. Note the 'new' location of C after MY.

11.9 Set normal or partial display mode

When $N/\bar{P} = 1$, the PCF8813 can operate only as a 67 + 1 row driver operating with a 1 : 68 multiplex rate. When $N/\bar{P} = 0$, the driver is used in free programmable multiplex rate where up to eight different multiplex rates can be selected in steps of 8, depending on the mask register value M[7:0]. When the PCF8813 is operating in FPMR mode, only the first 64 rows plus the icon row are available to the user.

Table 12 Normal or partial mode display

| N/P | ACTION |
|-----|---|
| 0 | partial mode display: 65 rows available |
| 1 | normal mode display: 68 rows available |

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11.10 Free programmable multiplex rate

The free programmable multiplex rate concept allows the user to limit the number of rows selected to groups of eight. Any, or all of these groups of rows can be enabled or disabled. The mask register command (M[7:0]) allows the user to turn-on or turn-off blocks of eight rows.

Each mask value controls a block of eight rows, thus in partial mode the maximum number of rows available is 64 plus the icon row. A logic 1 in the mask register enables the rows available within that block of rows, and a logic 0 disables them.

The mask register causes the row counter to count eight bits and then jump to the next enabled 8-bit group. For example, if the mask register value is 00001101, then the rows available will be 0 to 7, 16 to 23, 24 to 31 and 67.

Rows 8 to 15 and 32 to 63 have been skipped. This information is also mapped to the RAM so that only the contents of active rows are displayed.

Table 13 Range of free programmable multiplex rates

| MASK REGISTER | ROWS AVAILABLE |
|---------------|-----------------------|
| M0 | R0 to R7 + icon row |
| M1 | R8 to R15 + icon row |
| M2 | R16 to R23 + icon row |
| M3 | R24 to R31 + icon row |
| M4 | R32 to R39 + icon row |
| M5 | R40 to R47 + icon row |
| M6 | R48 to R55 + icon row |
| M7 | R56 to R63 + icon row |

Table 14 Examples of display normal driving mode and partial display driving mode

| MASK REGISTER | MASK VALUE | ROW SEQUENCE | NORMAL DISPLAY |
|--|------------|---------------|---------------------|
| $\overline{N/P} = 1$ (the mask value is don't care when $\overline{N/P} = 1$ because all rows are enabled) | | | |
| M0 | 1 | 0 to 7 | battery status: XXX |
| M1 | 0 | 8 to 15 | address book |
| M2 | 0 | 16 to 23 | connection time |
| M3 | 1 | 24 to 31 | network: YYY |
| M4 | 0 | 32 to 39 | reception strength |
| M5 | 0 | 40 to 47 | 2 June; 15:25 |
| M6 | 0 | 48 to 55 | |
| M7 | 1 | 56 to 63 | keyboard locked |
| not available in mask register | | 64 to 66 | |
| not available in mask register | | 67 (icon row) | |
| $\overline{N/P} = 0$ | | | |
| M0 | 1 | 0 to 7 | battery status: XXX |
| M1 | 0 | 8 to 15 | |
| M2 | 0 | 16 to 23 | |
| M3 | 1 | 24 to 31 | network: YYY |
| M4 | 0 | 32 to 39 | |
| M5 | 0 | 40 to 47 | |
| M6 | 0 | 48 to 55 | |
| M7 | 1 | 56 to 63 | keyboard locked |
| not available in mask register | | 67 (icon row) | |

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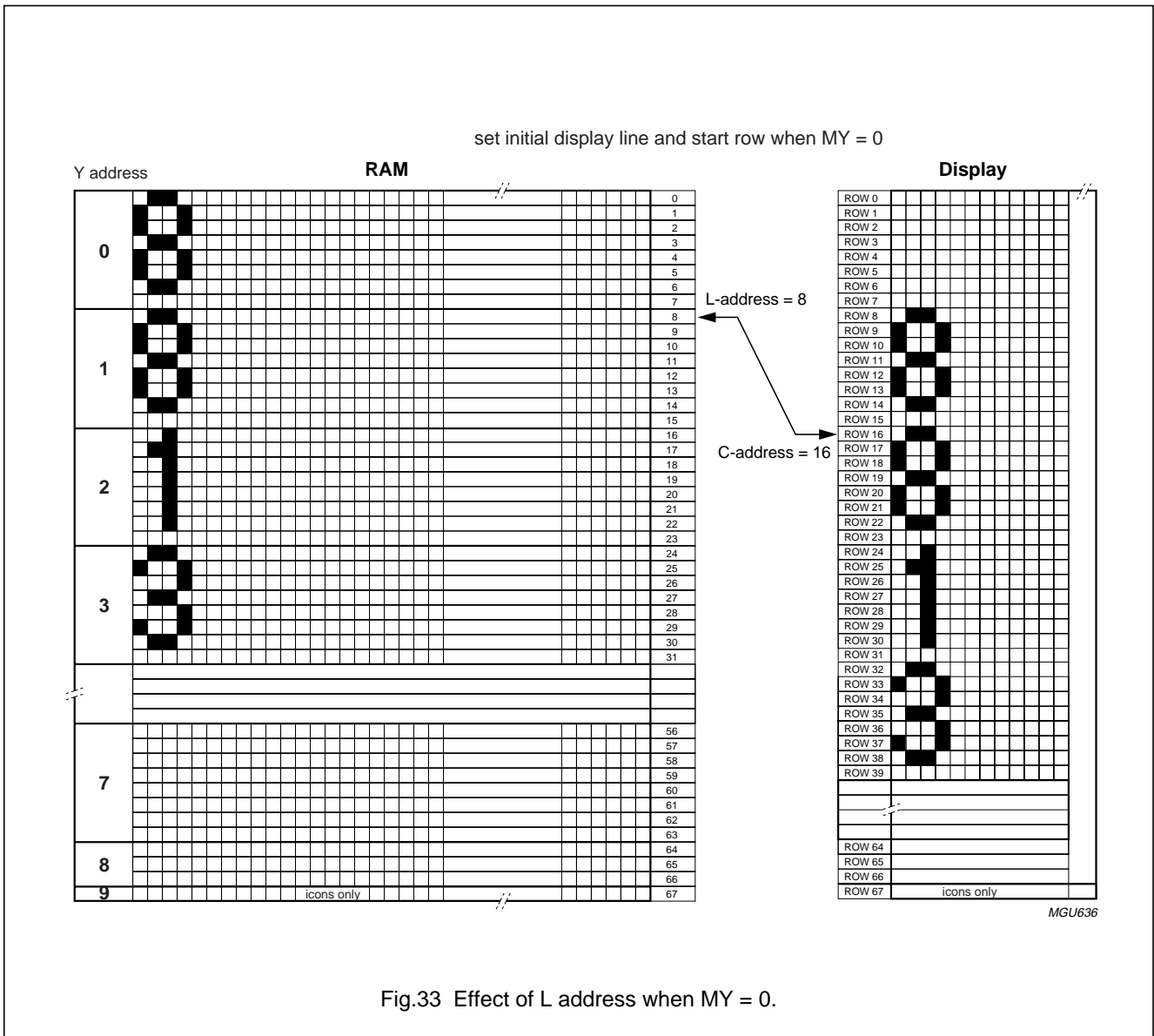


Fig.33 Effect of L address when MY = 0.

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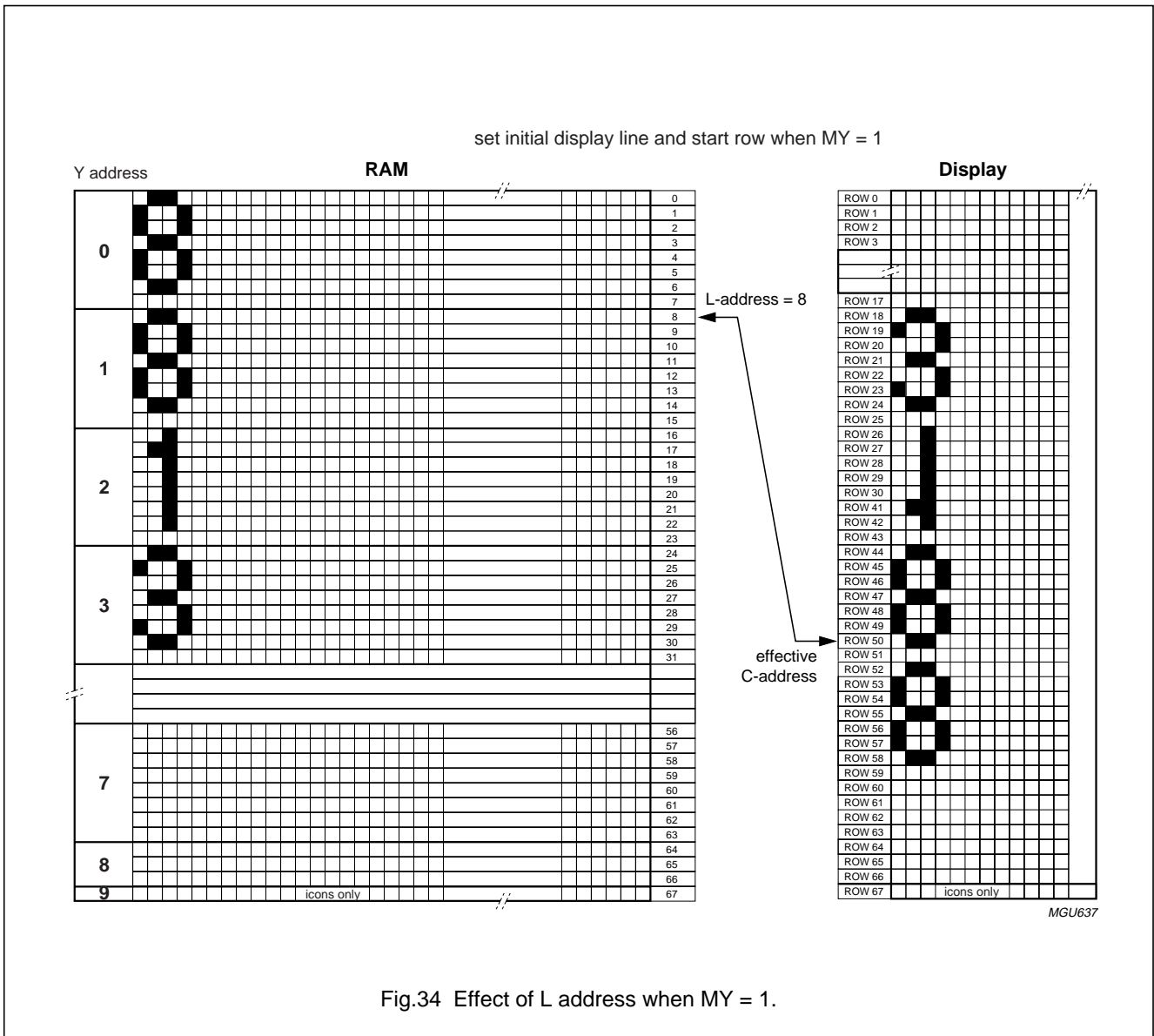


Fig.34 Effect of L address when MY = 1.

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11.11 Set HV generator stages

The PCF8813 incorporates a software-configurable voltage multiplier. After reset (\overline{RES}) the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the set HVgen stages command bits S[1:0].

11.12 Bias system

The bias voltage levels are set in the ratio of R - R - nR - R - R giving a $1/(n + 4)$ bias system. Different multiplex rates require different n factors. This is programmed by BS[2:0] (see Table 15).

For multiplex rates of 1 : 68 the optimum bias value n is given by: $n = \sqrt{68} - 3 = 5.246 = 5$ resulting in $1/9$ bias.

Changing the bias system from the optimum value will have a consequence for the contrast and viewing angle. One reason to depart from the optimum would be to reduce the required operating voltage. A compromise between contrast and operating voltage must be found for any particular application.

Table 15 Bias system programming

| BS[2] | BS[1] | BS[0] | n | RECOMMENDED MULTIPLEX RATES |
|-------|-------|-------|---|-----------------------------|
| 0 | 0 | 0 | 7 | 1 : 100 |
| 0 | 0 | 1 | 6 | 1 : 80 |
| 0 | 1 | 0 | 5 | 1 : 65 or 1 : 67 |
| 0 | 1 | 1 | 4 | 1 : 48 |
| 1 | 0 | 0 | 3 | 1 : 34 or 1 : 40 |
| 1 | 0 | 1 | 2 | 1 : 24 |
| 1 | 1 | 0 | 1 | 1 : 18 or 1 : 16 |
| 1 | 1 | 1 | 0 | 1 : 10, 1 : 9 or 1 : 8 |

Table 16 LCD bias voltage

| SYMBOL | BIAS VOLTAGES | BIAS VOLTAGES FOR $1/9$ BIAS |
|-------------------|-----------------------|------------------------------|
| V1 | V_{LCD} | V_{LCD} |
| V2 | $\frac{(n+3)}{(n+4)}$ | $8/9 \times V_{LCD}$ |
| V3 | $\frac{(n+2)}{(n+4)}$ | $7/9 \times V_{LCD}$ |
| V4 ⁽¹⁾ | $\frac{2}{(n+4)}$ | $2/9 \times V_{LCD}$ |
| V5 ⁽²⁾ | $\frac{1}{(n+4)}$ | $1/9 \times V_{LCD}$ |
| V6 | V_{SS} | V_{SS} |

Notes

- Operation of bias level V4 is given for $V4 > V_{SS} + 0.9$ V. For higher multiplex rates, V_{LCD} has to be selected accordingly.
- For multiplex rates equal to or lower than 1 : 24 ($n = 2$) operation of the bias level V5 is limited to voltages $V5 < V_{DD2,3} - 1.1$ V. V_{LCD} has to be selected accordingly.

The operating voltage can be set by software through the interface. The binary number V_{OP} representing the operating voltage can be set according to the following formula:

$$V_{OP} = V_{CAL}[4:0] + V_{PR*}$$

Where:

V_{OP} is an 8-bit unsigned number used internally for generation of the LCD supply voltage V_{LCD}

V_{CAL} is a 5-bit twos complement number set by the module maker; see Table 17

V_{PR} is an 8-bit unsigned number composed of PRS and V_{PR*} set by an interface command.

The corresponding voltage at the reference temperature, T_{CUT} , can be calculated as:

$$V_{LCD(T_{cut})} = (a + V_{OP} \times b)$$

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The generated voltage at V_{LCD} is dependent on the temperature, programmed temperature coefficient (TC) and the programmed voltage at the reference temperature (T_{CUT}):

$$V_{LCD} = [a + V_{OP} \times b] \times [1 + TC \times (T - T_{CUT})]$$

T_{CUT} and voltages a and b for each temperature coefficient are quoted in Table 17. The maximum voltage that can be generated is dependent on the voltage of V_{DD2} and the display load current.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} , the user must ensure that while setting the V_{PR}

register and selecting the temperature compensation, under all conditions and including all tolerances the V_{LCD} maximum limit of 9.0 V will never be exceeded.

For a particular liquid crystal, the optimum V_{LCD} can be calculated for a given multiplex rate. For 1 : 68, the optimum operating voltage of the liquid crystal can be calculated as;

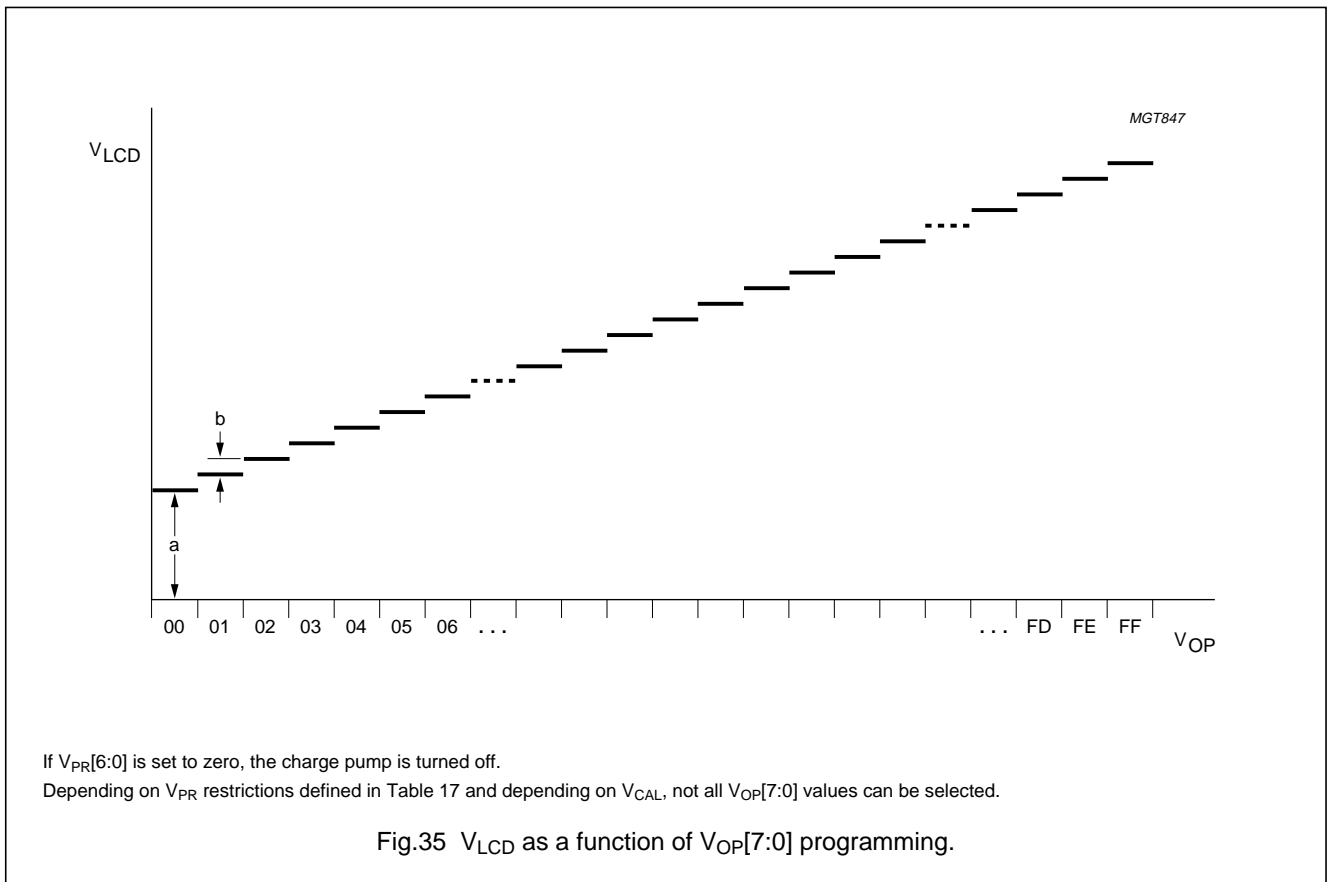
$$V_{LCD} = \frac{1 + \sqrt{68}}{\sqrt{2} \times \left(1 - \frac{1}{\sqrt{68}}\right)} \times V_{th} = 6.98 \times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal used.

Table 17 Parameters of HV generator programming (typical values)

Nominal temperature = 27 °C; temperature coefficients calculated at nominal $V_{LCD} = 8.6$ V.

| SYMBOL | PARAMETER | TC0 | TC1 | TC2 | TC3 | UNIT |
|-----------|-------------------------------|------|-------|-------|-------|------|
| a | first level V_{LCD} voltage | 4.57 | 4.27 | 4.01 | 3.84 | V |
| b | programmed voltage step | 30.5 | 28.5 | 26.7 | 25.6 | mV |
| T_{CUT} | reference temperature | 27 | 27 | 27 | 27 | °C |
| TC | temperature coefficient | 0.00 | -0.25 | -0.48 | -0.64 | mV/K |

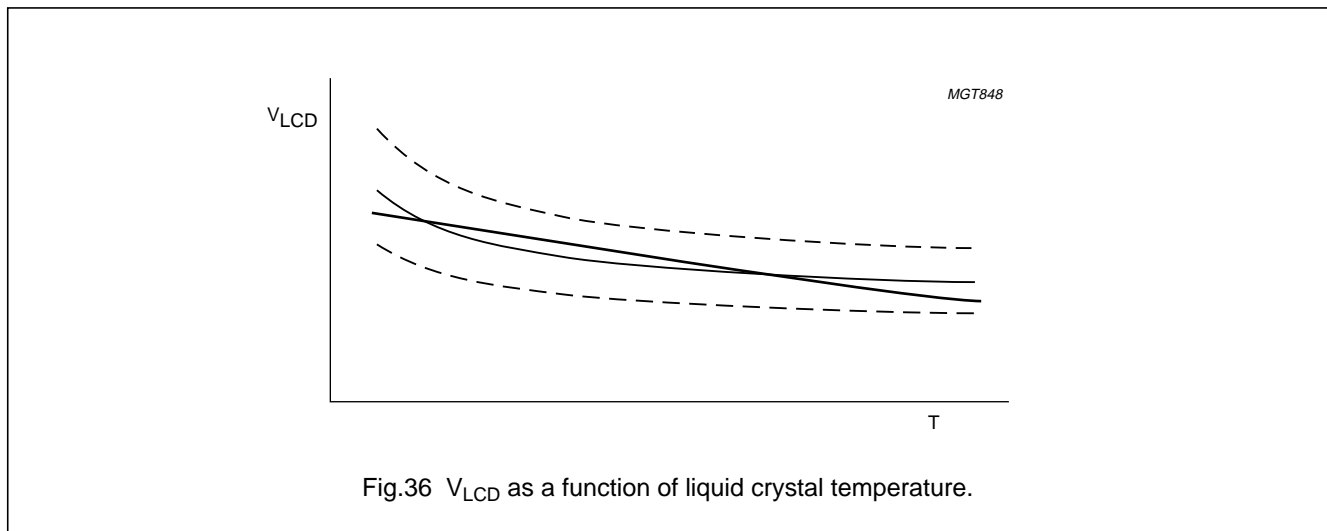


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12 TEMPERATURE COMPENSATION

Due to the temperature dependency of the liquid crystal viscosity, the LCD controlling voltage V_{LCD} must be increased at lower temperatures to maintain optimum contrast. Figure 36 shows V_{LCD} for high multiplex rates. In the PCF8813 the temperature coefficient to be applied to V_{LCD} can be selected from four values by setting bits TC[1:0].

**13 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); see notes 1 and 2

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|--------------------|---|------|----------------|------|
| V_{DD1} | supply voltage | -0.5 | +6.5 | V |
| V_{DD2}, V_{DD3} | supply voltage (voltage multiplier); see note 3 | -0.5 | +4.5 | V |
| V_{LCD} | LCD supply voltage | -0.5 | +9.0 | V |
| V_I | input voltage (any pad) | -0.5 | $V_{DD} + 0.5$ | V |
| I_{SS} | ground supply current | -50 | +50 | mA |
| I_I, I_O | DC input or output current | -10 | +10 | mA |
| P_{tot} | total power dissipation | - | 300 | mW |
| P_O | power dissipation per output | - | 30 | mW |
| T_{stg} | storage temperature | -65 | +150 | °C |
| T_j | junction temperature | - | 150 | °C |

Notes

- Stresses above those listed under limiting values may cause permanent damage to the device.
- Parameters are valid over operating temperature range unless otherwise specified; all voltages are with respect to V_{SS} unless otherwise specified.
- V_{DD2} and V_{DD3} are always equal.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

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15 DC CHARACTERISTICS $V_{DD1} = 1.7$ to 3.3 V; $V_{SS} = 0$ V; $V_{LCD} = 3.0$ to 9.0 V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|---|------------------------------------|-------------|-------|-------------|------------|
| V_{DD1} | supply voltage (logic circuits) | | 1.7 | – | 3.3 | V |
| V_{DD2}, V_{DD3} | supply voltage (voltage multiplier) | note 1 | 2.4 | – | 4.5 | V |
| V_{LCDIN} | LCD supply voltage input | | 3.0 | – | 9.0 | V |
| V_{LCDOUT} | generated LCD supply voltage | note 2 | 4.5 | – | 9.0 | V |
| $V_{LCD(tol)}$ | tolerance of generated LCD supply voltage | note 3 | –70 | – | +70 | mV |
| $I_{DD(tot)}$ | total supply current ($I_{DD1} + I_{DD2} + I_{DD3}$) | normal mode; notes 4, 5, 6 | – | 100 | 300 | μ A |
| | | Power-down mode; note 7 | – | 0.5 | 10 | μ A |
| I_{DD1} | supply current | external V_{LCD} ; notes 4, 6, 8 | – | 10 | 35 | μ A |
| I_{LCD} | LCD supply current | external V_{LCD} ; notes 4, 6, 8 | – | 30 | – | μ A |
| Logic circuits | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{OL} = 0.5$ mA | V_{SS} | – | $0.2V_{DD}$ | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -0.5$ mA | $0.8V_{DD}$ | – | V_{DD} | V |
| V_{IL} | LOW-level input voltage | | V_{SS} | – | $0.2V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.8V_{DD}$ | – | V_{DD} | V |
| I_L | leakage current | $V_I = V_{DD}$ or V_{SS} | –1 | – | +1 | μ A |
| Column and row outputs | | | | | | |
| R_{col} | column output resistance C0 to C101 | $V_{LCD} = 7.6$ V; note 9 | – | 5 | 20 | k Ω |
| R_{row} | row output resistance R0 to R67 | $V_{LCD} = 7.6$ V; note 9 | – | 5 | 20 | k Ω |
| $V_{col(tol)}$ | bias tolerance C0 to C101 | note 9 | –100 | 0 | +100 | mV |
| $V_{row(tol)}$ | bias tolerance R0 to R67 | note 9 | –100 | 0 | +100 | mV |
| LCD supply voltage generator | | | | | | |
| TC | V_{LCD} temperature compensation | $V_{LCD(nom)} = 8.6$ V | – | 0.00 | – | mV/K |
| | temperature coefficient 0 | | – | –0.23 | – | mV/K |
| | temperature coefficient 1 | | – | –0.48 | – | mV/K |
| | temperature coefficient 2 | | – | –0.64 | – | mV/K |

Notes

- V_{DD2} and V_{DD3} are always equal.
- The maximum possible V_{LCD} voltage that may be generated depends on voltage, temperature and load (display).
- Valid for the temperature, V_{PR} and TC values used at calibration.
- Normal mode and internal clock.
- Conditions: $V_{DD1} = 1.8$ V; $V_{DD2} = 2.70$ V; $V_{LCD} = 7.6$ V; voltage multiplier = $4 \times V_{DD2}$; bias system $1/9$; inputs at V_{DD1} or V_{SS} ; V_{LCD} generation = internal; V_{LCD} output loaded by 10 μ A; $T_{amb} = 25$ °C.
- $f_{INTCLK} = 0$ (no data bus clock).
- Power-down mode; during Power-down all static currents are switched off.

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8. V_{LCD} external voltage applied to V_{LCDIN} and $V_{LCDSENSE}$ inputs; V_{LCDOUT} disconnected; V_{PR} and PC set to 0 (charge pump off); display load current is not transmitted to I_{DD} .
9. Load current = 10 μ A; outputs tested one at a time.

16 AC CHARACTERISTICS

$V_{DD1} = 1.7$ to 3.3 V; $V_{SS} = 0$ V; $V_{LCD} = 3.0$ to 9.0 V; $T_{amb} = -40$ to $+85$ °C; all timings specified are based on 20% to 80% of V_{DD} with an input voltage swing of V_{SS} to V_{DD} ; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|------------------|----------|----------|----------|
| f_{ext} | external clock frequency | note 1 | 20 | 38 | 65 | kHz |
| f_{frame} | frame frequency | internal oscillator note 2 note 3 | 56 62 | 66 69 | 76 76 | Hz Hz |
| t_{VHRL} | V_{DD} on to \overline{RES} LOW time | see Fig.37 | 0 ⁽⁴⁾ | – | 1 | μ s |
| t_{RW} | reset pulse width LOW time | see Fig.37 | 500 | – | – | ns |
| $t_{R(oper)}$ | end of reset pulse to interface operational | see Fig.37 | 1000 | – | – | ns |
| 6800-type parallel bus; $V_{DD1} = 1.8$ to 3.3 V; see Figs 38 and 39 | | | | | | |
| t_{DCSU} | data/ $\overline{command}$ set-up time | | 0 | – | 25 | ns |
| t_{DCHD} | data/ $\overline{command}$ hold time | | 0 | – | – | ns |
| $T_{DS(cyc)}$ | data strobe cycle time | | 1000 | – | – | ns |
| t_{DSL} | data strobe LOW time | | 300 | – | – | ns |
| t_{DSH} | data strobe HIGH time | | 300 | – | – | ns |
| t_{RWSU} | read/ \overline{write} set-up time | | 0 | – | – | ns |
| t_{RWHD} | read/ \overline{write} hold time | | 0 | – | – | ns |
| t_{ESU} | chip enable set-up time | | 0 | – | – | ns |
| t_{EHD} | chip enable hold time | | 0 | – | – | ns |
| t_{DATSU} | data set-up time | | 80 | – | – | ns |
| t_{DATHD} | data hold time | | 30 | – | – | ns |
| $t_{DATAACC}$ | output access time | | – | – | 280 | ns |
| t_{DATOH} | output disable time | | 10 | – | 200 | ns |
| 8080-type parallel bus; $V_{DD1} = 1.8$ to 3.3 V; see Fig.40 | | | | | | |
| t_{DCSU} | data/ $\overline{command}$ set-up time | | 0 | – | 25 | ns |
| t_{DCHD} | data/ $\overline{command}$ hold time | | 0 | – | – | ns |
| $T_{DS(cyc)}$ | data strobe cycle time | | 1000 | – | – | ns |
| t_{DSLr} | data strobe LOW time (read) | | 120 | – | – | ns |
| t_{DSLw} | data strobe LOW time (write) | | 240 | – | – | ns |
| t_{DSHR} | data strobe HIGH time (read) | | 120 | – | – | ns |
| t_{DSHW} | data strobe HIGH time (write) | | 120 | – | – | ns |
| t_{DATSU} | data set-up time | | 80 | – | – | ns |
| t_{DATHD} | data hold time | | 30 | – | – | ns |
| $t_{DATAACC}$ | output access time | | – | – | 280 | ns |
| t_{DATOH} | output disable time | | 10 | – | 200 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|------------|------|------|------|----------|
| 3-line and 4-line SPI and serial interface; $V_{DD1} = 1.8$ to 3.3 V; Figs 41 to 44; note 5 | | | | | | |
| f_{SCLK} | SCLK frequency | | – | – | 9 | MHz |
| T_{cyc} | SCLK cycle time | | 111 | – | – | ns |
| t_{PWH1} | SCLK pulse width HIGH | | 45 | – | – | ns |
| t_{PWL1} | SCLK pulse width LOW | | 45 | – | – | ns |
| t_{PWH2} | \overline{SCE} minimum HIGH time | | 50 | – | – | ns |
| t_{S1} | SDATA set-up time | | 50 | – | – | ns |
| t_{H1} | SDATA hold time | | 50 | – | – | ns |
| t_{S2} | \overline{SCE} set-up time | | 60 | – | – | ns |
| t_{H2} | \overline{SCE} hold time | | 45 | – | – | ns |
| t_{S3} | data/command set-up time | | 50 | – | – | ns |
| t_{H3} | data/command hold time | | 50 | – | – | ns |
| t_1 | SDOUT access time | | – | – | 80 | ns |
| t_2 | SDOUT disable time | note 6 | – | – | 80 | ns |
| t_3 | \overline{SCE} hold time | | 50 | – | – | ns |
| t_4 | SDOUT disable time | note 7 | – | – | 80 | ns |
| C_b | capacitive load for SDOUT | note 8 | – | – | 30 | pF |
| R_b | series resistance for SDOUT | note 8 | – | – | 500 | Ω |
| I²C-bus interface in Fast-mode; $V_{DD1} = 1.7$ to 3.3 V; Fig.45 | | | | | | |
| f_{SCL} | SCL clock frequency | | 0 | – | 400 | kHz |
| t_{LOW} | SCL clock low period | | 1.3 | – | – | μ s |
| t_{HIGH} | SCL clock high period | | 0.6 | – | – | μ s |
| $t_{SU;DAT}$ | data set-up time | | 100 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | – | 0.9 | μ s |
| C_b | capacitive load represented by each bus line | | – | – | 400 | pF |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 0.6 | – | – | μ s |
| $t_{HD;STA}$ | START condition hold time | | 0.6 | – | – | μ s |
| $t_{SU;STO}$ | set-up time for STOP condition | | 0.6 | – | – | μ s |
| t_{SP} | tolerable spike width on bus | note 9 | – | – | 50 | ns |
| I²C-bus interface in Hs-mode; $V_{DD1} = 1.7$ to 3.3 V; Fig.46 | | | | | | |
| f_{SCLH} | SCLH clock frequency | | 0 | – | 3.4 | MHz |
| $t_{SU;STA}$ | set-up time (repeated) START condition | | 160 | – | – | ns |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 160 | – | – | ns |
| t_{LOW} | LOW period of the SCLH clock | | 160 | – | – | ns |
| t_{HIGH} | HIGH period of the SCLH clock | | 60 | – | – | ns |
| $t_{SU;DAT}$ | data set-up time | | 10 | – | – | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------|---|-----------------------------------|------|------|------|------|
| t _{HD;DAT} | data hold time | | 0 | – | 70 | ns |
| t _{SU;STO} | set-up time for STOP condition | | 160 | – | – | ns |
| C _b | capacitive load for SDAH and SCLH lines | total capacitance of one bus line | – | – | 100 | pF |
| | capacitive load for SDAH + SDA line and SCLH + SCL line | | – | – | 400 | pF |
| t _{SP} | tolerable spike width on bus | note 9 | – | – | 5 | ns |

Notes

- $f_{\text{frame}} = \frac{f_{\text{ext}}}{n}$: (n depends on the multiplex rate, see Table 18).
- V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = 3.0 to 9.0 V; T_{amb} = –40 to +85 °C, all MUX settings.
- V_{DD1} = 2.4 V to 3.0 V; T_{amb} = –20 °C to +70 °C; MUX = 68.
- $\overline{\text{RES}}$ may be LOW before V_{DD} on.
- Maximum values are for f_{SCLK} = 9 MHz. Series resistance includes ITO track + connector resistance + printed-circuit board.
- SDOUT disable time for SPI 3-line or 4-line interface.
- SDOUT disable time for serial 3-line interface.
- Typical conditions: V_{DD1} = 2.8 V, T_{amb} = 20 °C, MUX = 68; f_{frame} = 70 ± 3.4 Hz.
- Inputs SDAH and SCLH are filtered and will reject spikes on the bus lines with a width of less than t_{SW(max)}.

Table 18 Value of n as a function of multiplex rate

| MULTIPLEX RATE | n |
|----------------|-----|
| 68 | 483 |
| 65 | 462 |
| 57 | 464 |
| 49 | 500 |
| 41 | 504 |
| 33 | 476 |
| 25 | 468 |
| 17 | 505 |
| 9 | 500 |

(67 + 1) × 102 pixels matrix LCD driver

PCF8813

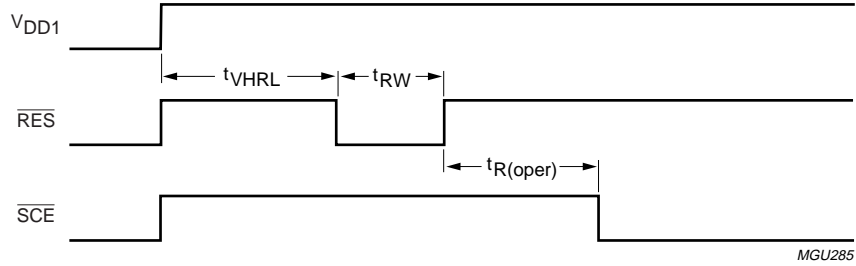


Fig.37 Reset timing.

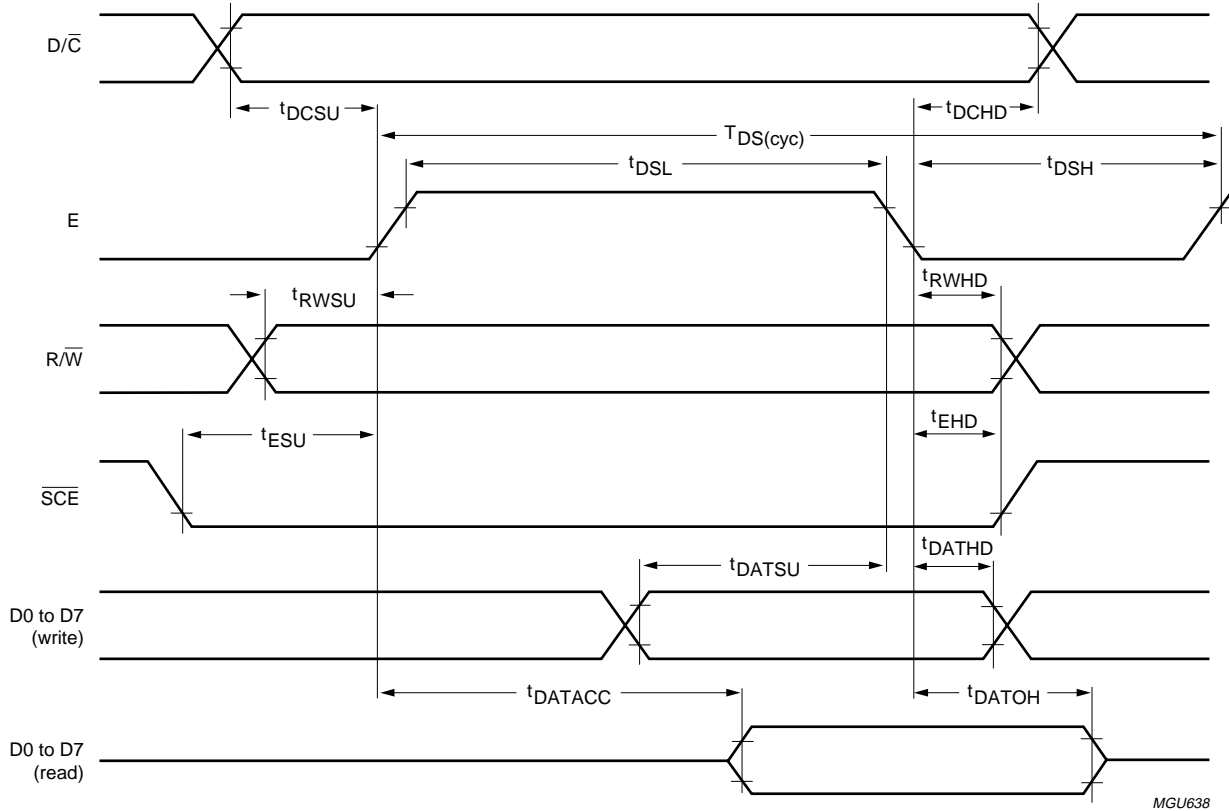


Fig.38 Parallel interface timing (6800-type) with clocking performed by enable input (E).

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PCF8813

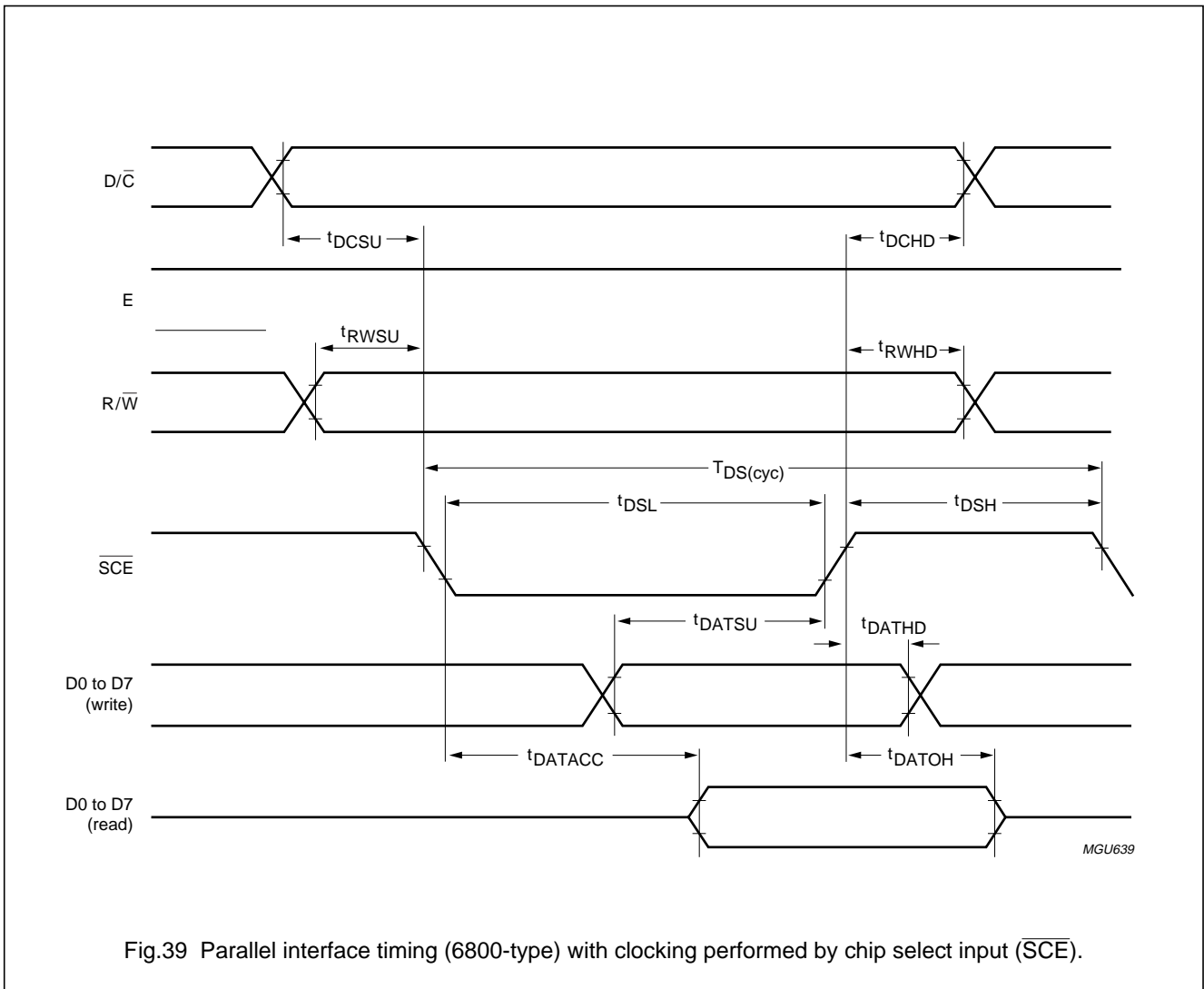


Fig.39 Parallel interface timing (6800-type) with clocking performed by chip select input (\overline{SCE}).

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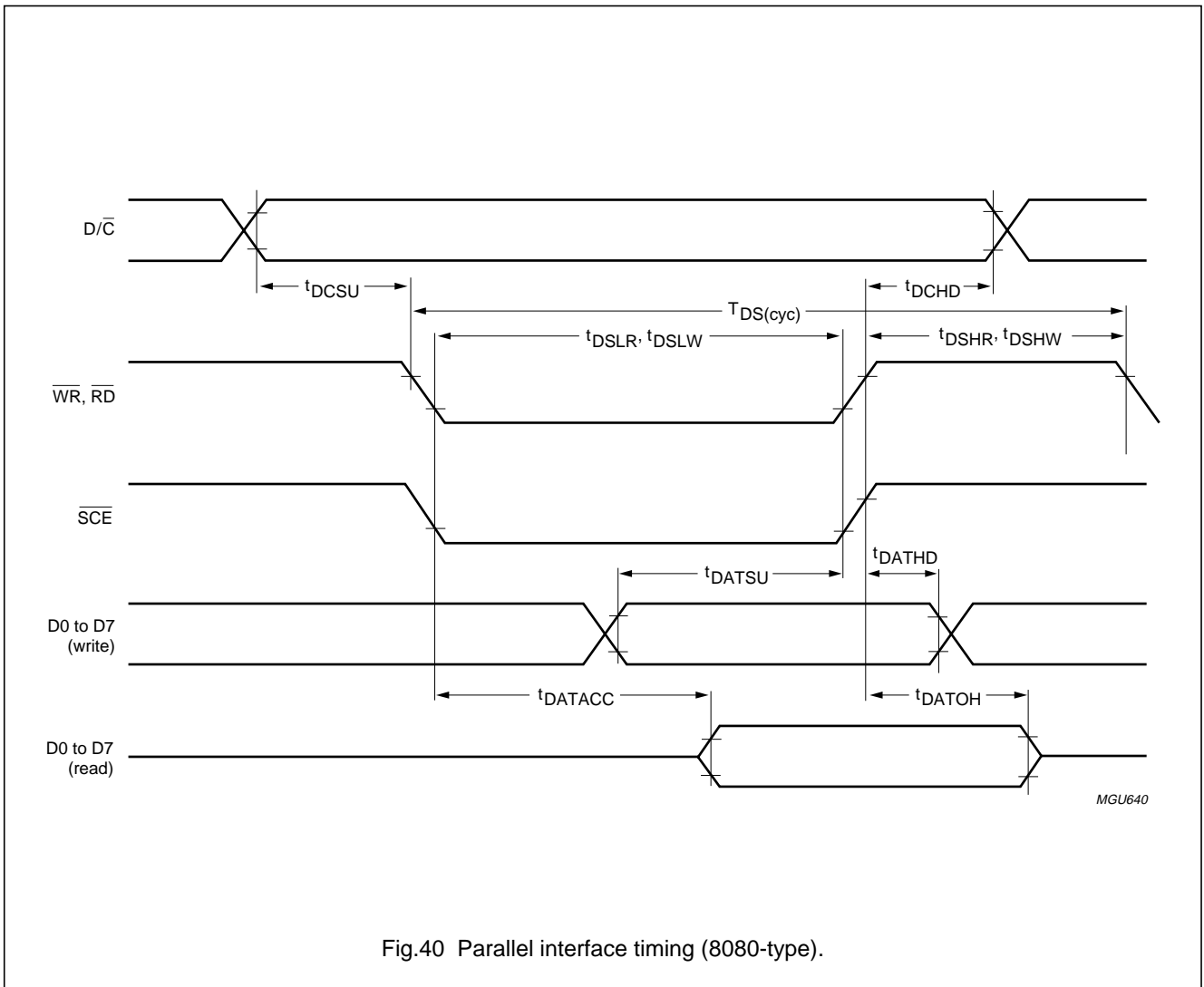


Fig.40 Parallel interface timing (8080-type).

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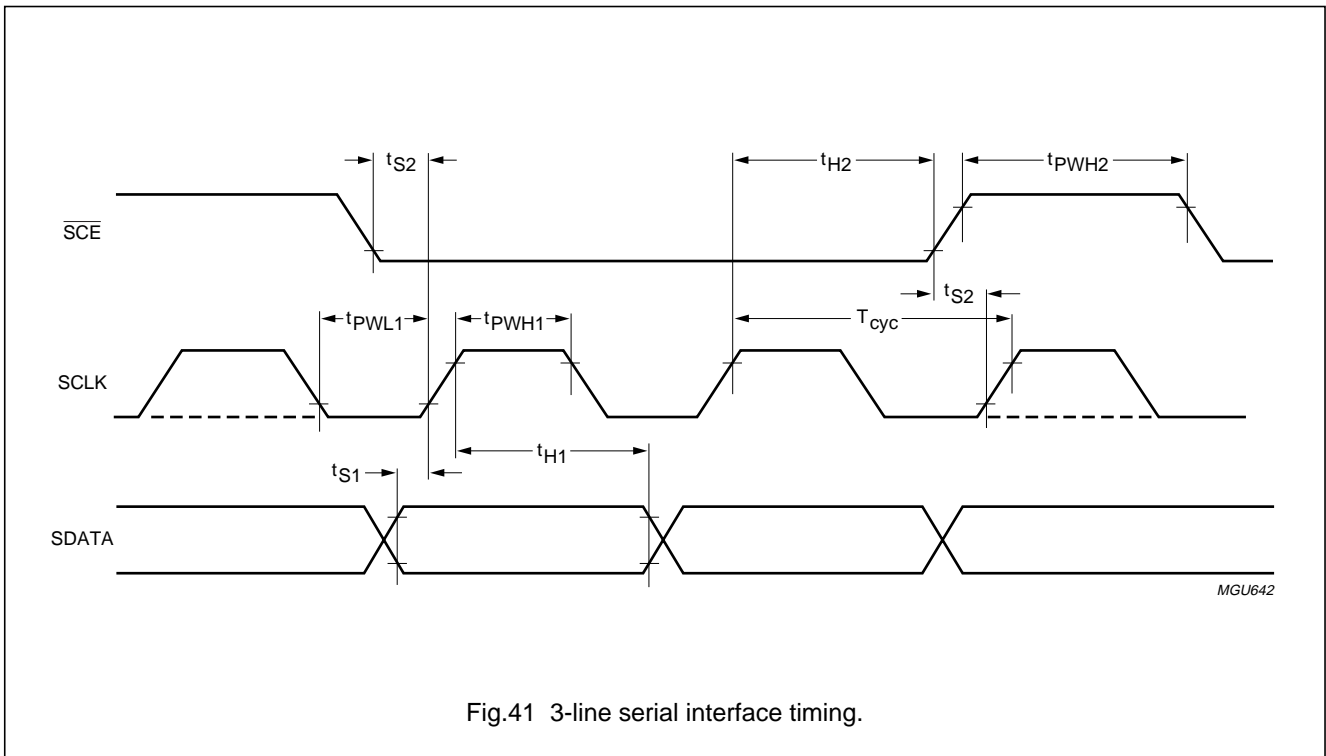


Fig.41 3-line serial interface timing.

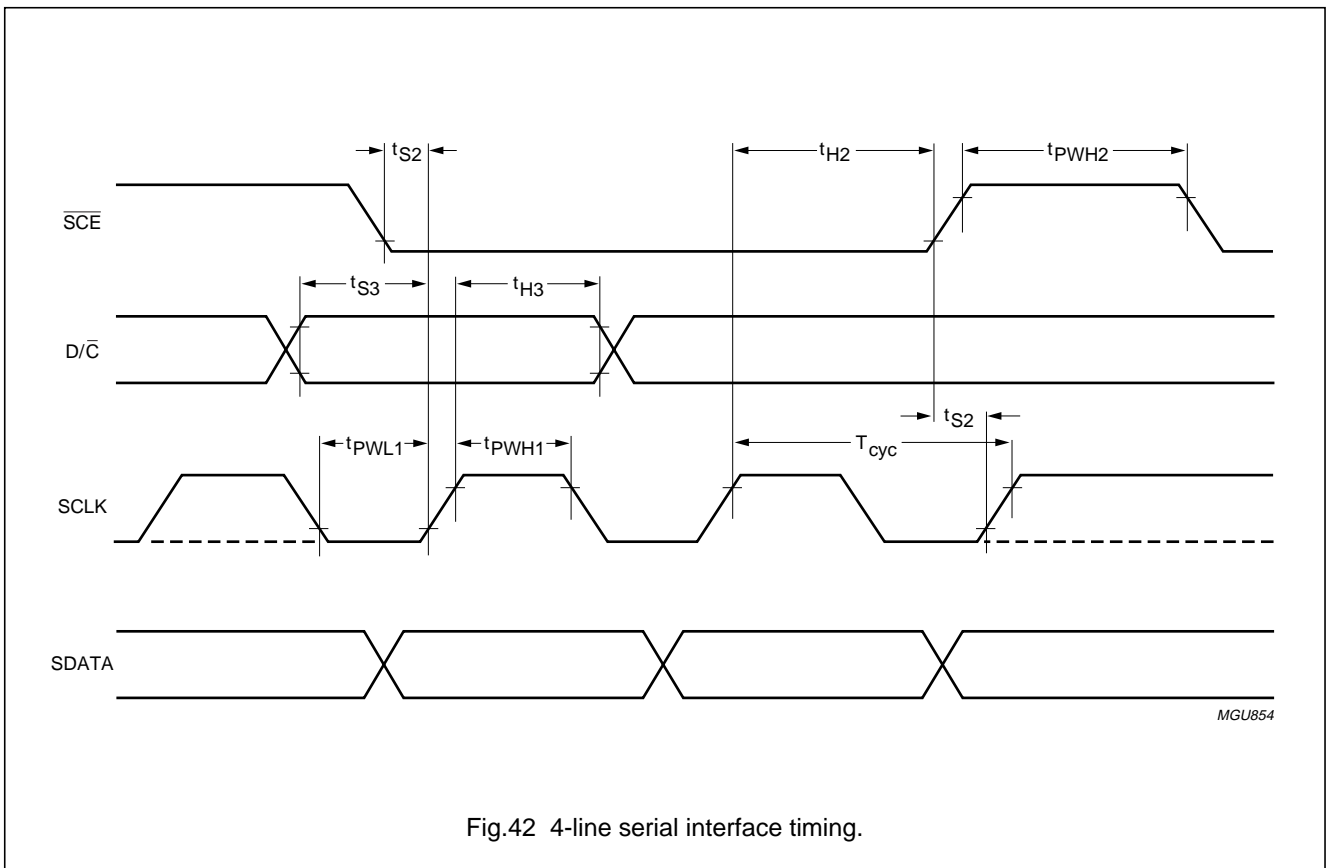
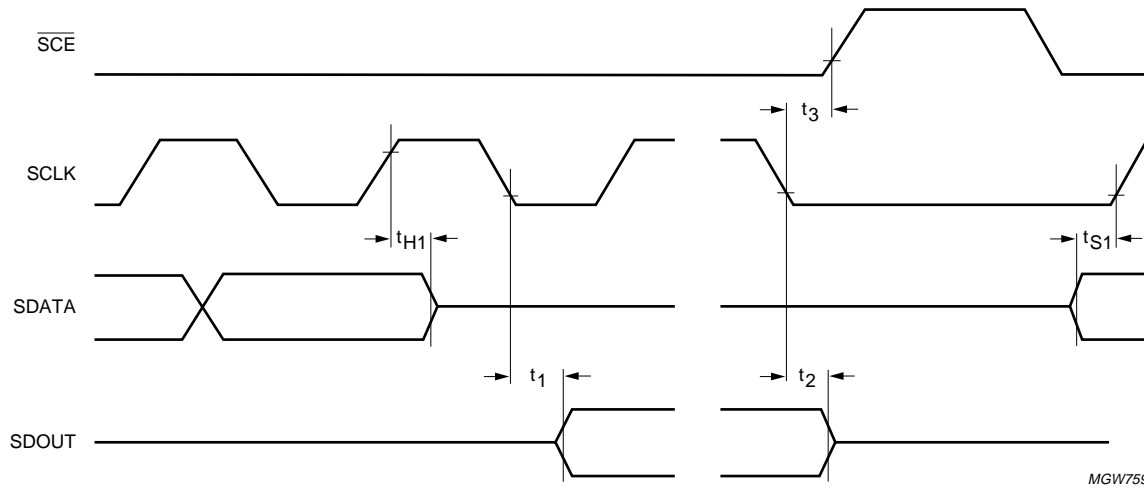


Fig.42 4-line serial interface timing.

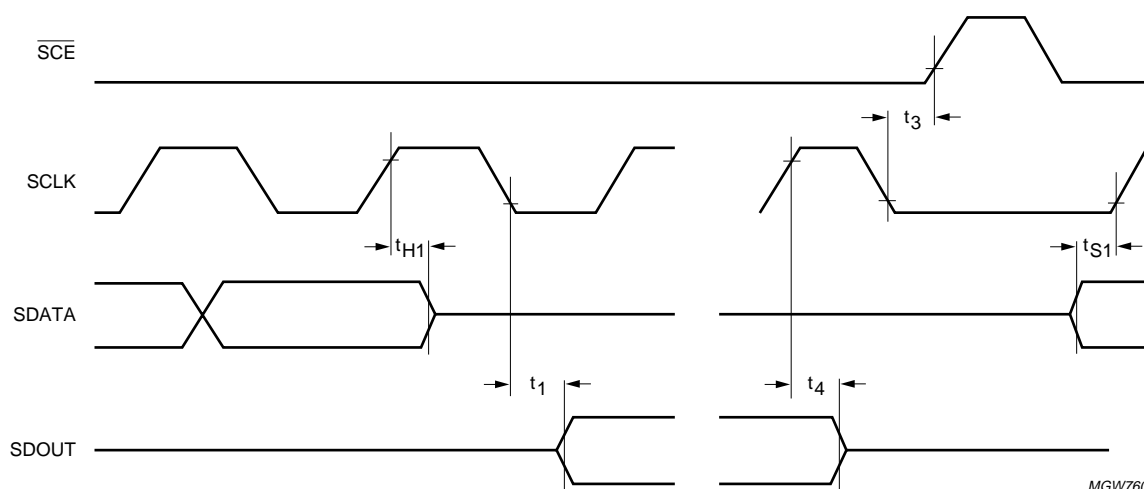
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MGW759

Fig.43 3-line and 4-line serial peripheral (SPI) interface timing (read mode).



MGW760

Fig.44 3-line serial interface timing (read mode).

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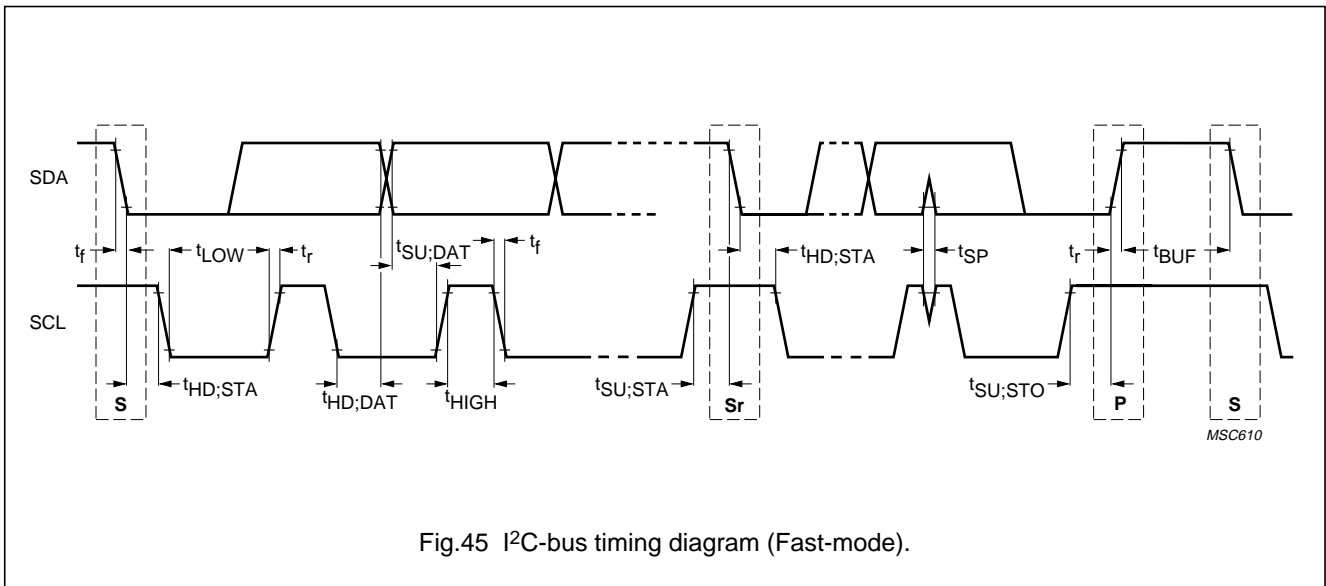


Fig.45 I²C-bus timing diagram (Fast-mode).

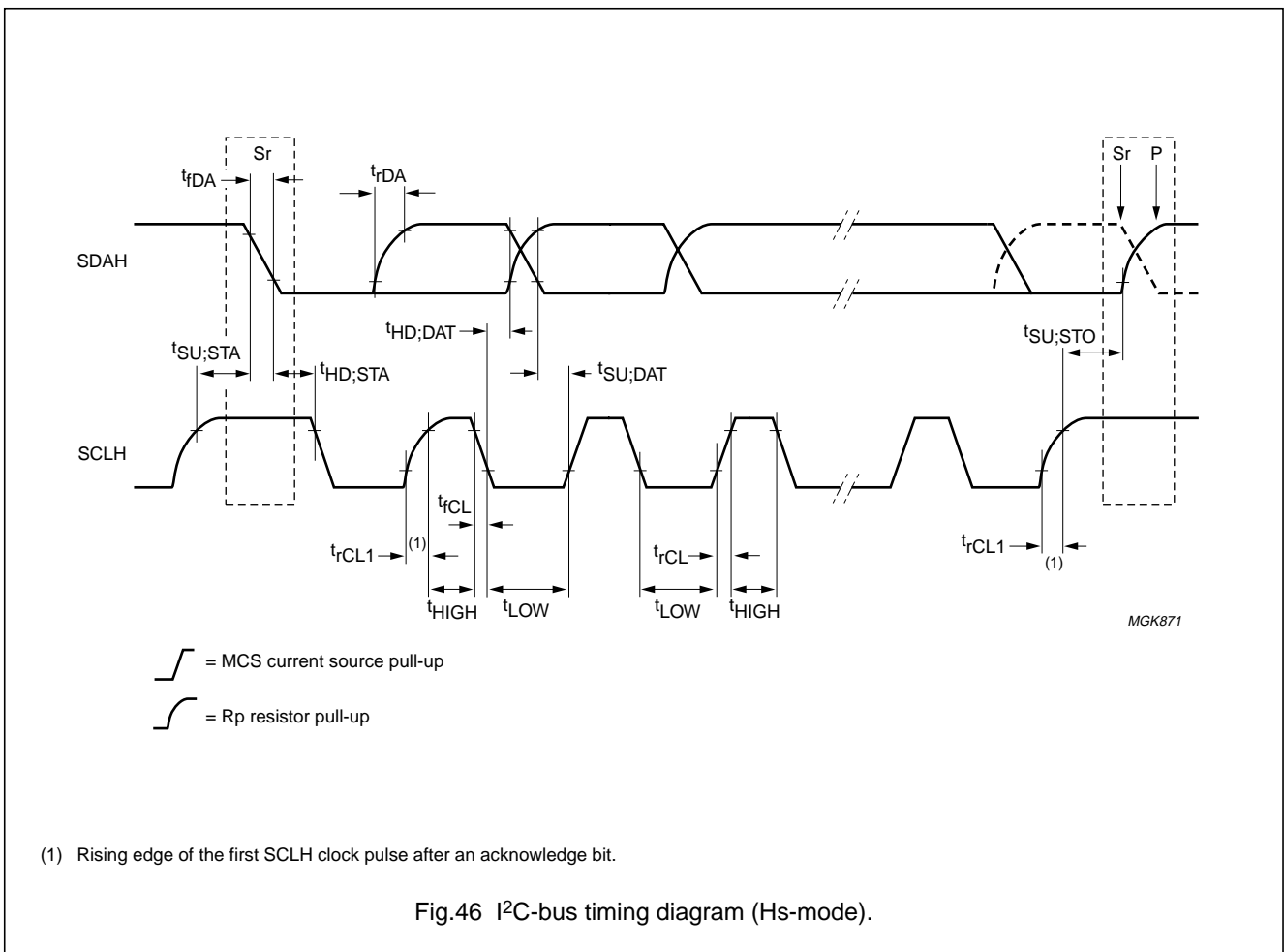


Fig.46 I²C-bus timing diagram (Hs-mode).

(67 + 1) × 102 pixels matrix LCD driver

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17 MODULE MAKER PROGRAMMING

One Time Programmable (OTP) technology has been implemented on the PCF8813. This enables the module maker to program some features of the PCF8813 after it has been assembled on an LCD module. Programming is made under the control of the interfaces and using the special pad V_OTPPROG. This pad must be made available on the module glass but does not need to be accessed by the set maker.

Module maker programming is an extension of the normal functions of the PCF8813 and is effective until specifically instructed otherwise with the disable OTP command.

The PCF8813 features three module maker programmable parameters:

- V_{LCD} calibration (5 bits)
- Manufacturer identity (3 bits)
- Seal bit (1-bit).

17.1 LCD voltage calibration

Referring to Fig.47, the V_{LCD} calibration parameter comprises a 5-bit code (V_{CAL}[4:0]). The code is implemented in twos complement notation giving a positive or negative offset to the V_{PR} register. The range of the V_{PR}[6:0] register is 0 to 127. The adder in the circuit takes this into account by having underflow and overflow protection added to it. In the event of an overflow, the output will be clamped to 255, and in the case of an underflow the output will be clamped to 0.

Given that

V_{OP} = V_{CAL} + V_{PR*}

and

V_{LCD} = a + V_{OP} × b |_{T(norm)}

V_{LCD} can be calculated using parameters a and b that are defined in Table 17. An example of the relationship between V_{CAL} code and the V_{LCD} calibration is shown in Table 19, where b is assumed to be 25.6 mV.

Possible values for V_{CAL} are given in Table 19. The default value for V_{CAL} when OTP is disabled is V_{CAL}[4:0] = 00000.

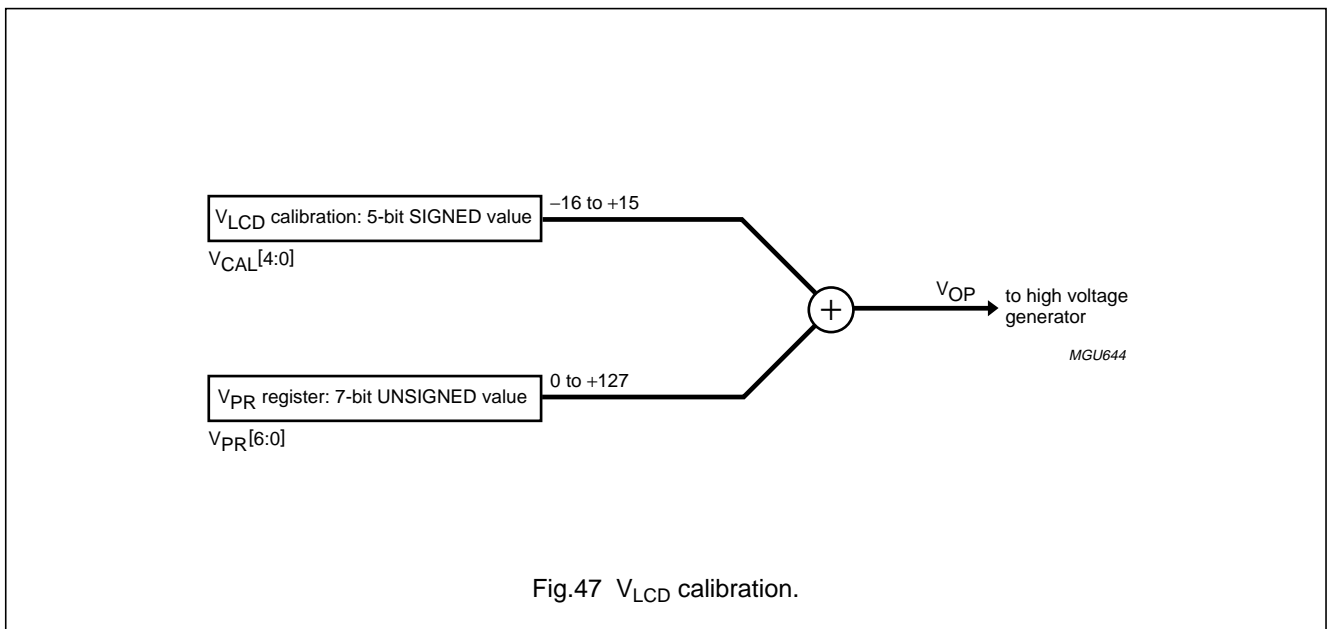


Fig.47 V_{LCD} calibration.

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Table 19 V_{CAL} codes and associated nominal calibration voltage when the temperature coefficient is set to TC3

| V_{CAL} | $V_{CAL}[4:0]$ | V_{LCD} CALIBRATION (mV) |
|-----------|----------------|----------------------------------|
| +0 | 00000 | 0 (default) |
| +1 | 00001 | +25.6 |
| +2 | 00010 | +51.2 |
| +3 | 00011 | +76.8 |
| +4 | 00100 | +102.4 |
| +5 | 00101 | +128.0 |
| +6 | 00110 | +153.6 |
| +7 | 00111 | +179.2 |
| +8 | 01000 | +204.8 |
| +9 | 01001 | +230.4 |
| +10 | 01010 | +256.0 |
| +11 | 01011 | +281.6 |
| +12 | 01100 | +307.2 |
| +13 | 01101 | +332.8 |
| +14 | 01110 | +358.4 |
| +15 | 01111 | +384.0 |
| -1 | 11111 | -25.6 |
| -2 | 11110 | -51.2 |
| -3 | 11101 | -76.8 |
| -4 | 11100 | -102.4 |
| -5 | 11011 | -128.0 |
| -6 | 11010 | -153.6 |
| -7 | 11001 | -179.2 |
| -8 | 11000 | -204.8 |
| -9 | 10111 | -230.4 |
| -10 | 10110 | -256.0 |
| -11 | 10101 | -281.6 |
| -12 | 10100 | -307.2 |
| -13 | 10011 | -332.8 |
| -14 | 10010 | -358.4 |
| -15 | 10001 | -384.0 |
| -16 | 10000 | -409.6 |

17.2 Manufacturer identity

The second OTP feature defines the manufacturer identity. A 3-bit code MF[2:0] is used to define this parameter. The default manufacturer identity is MF[2:0] = 000.

17.3 Seal bit

Module maker programming is performed in a special mode; the calibration mode MM. This mode is entered via the interface command, MM. To prevent wrongful programming, a seal bit prevents the device from entering the calibration mode. This seal bit, once programmed, cannot be reversed, thus further changes in programmed values are not possible. However it is possible to disable all programmed values by applying the disable OTP command.

Applying the programming voltages when not in MM mode will have no effect on the programmed values.

Table 20 Seal bit definition

| SEAL BIT | ACTION |
|----------|------------------------------------|
| 0 | possible to enter calibration mode |
| 1 | calibration mode disabled |

17.4 One time programming**17.4.1 ARCHITECTURE**

The OTP circuitry in the PCF8813 contains nine bits of data: five for V_{LCD} calibration, three for the manufacturer identity and one for the seal bit. The circuitry for 1-bit is called an OTP slice. Each OTP slice consists of two main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are accessible only through their shift register cells; both reading-from and writing-to the OTP cells are performed with the shift register cells, but only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Fig.48.

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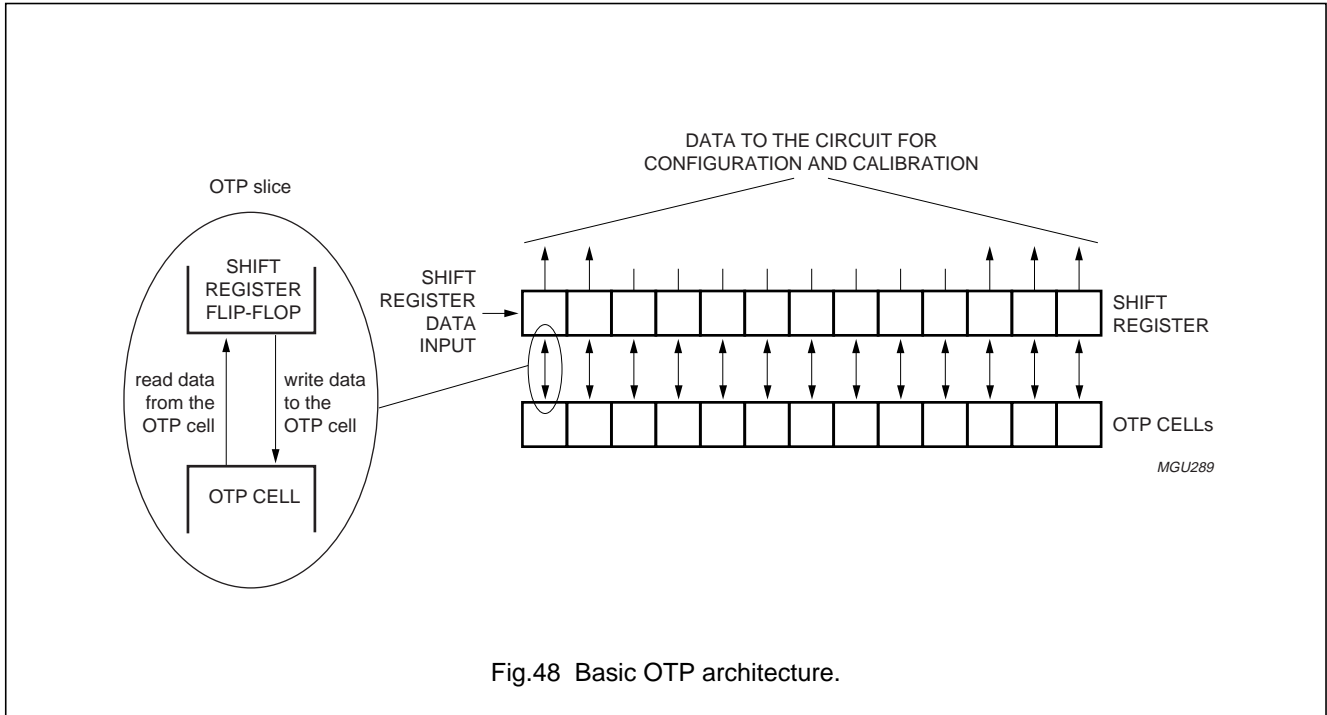


Fig.48 Basic OTP architecture.

17.4.2 OPERATIONS

The OTP architecture allows the following operations:

- The OTP circuit in the PCF8813 is initialized when a reset is initiated. After the reset initiation, OTP circuits can be disabled only by sending the disable OTP command.
- Reading data from the OTP cells. The content of the non-volatile OTP cells is transferred to the shift register where it may affect operation of the PCF8813.
- Writing data to the OTP cells. All 9 bits of data are shifted first into the shift register via the serial interface. Then the content of the shift register is transferred to the OTP cells (there are some limitations related to storing data in these cells; see Section 17.6).
- Checking calibration without writing to the OTP cells. Shifting data into the shift register allows the effects of the V_{LCD} voltage to be observed.

All OTP circuitry of the PCF8813 is enabled until the disable OTP command is given. Once enabled, the reading of data from the OTP cells is initiated by either:

- Exit from Power-down mode
- The Refresh command (power control). This command works only when the driver is not in Power-down.

In both cases, the time required for the reading operation to complete is up to 5 ms.

The shifting of data into the shift register is performed in the special mode MM. In the PCF8813, the MM mode is entered through the MM command. Once in the MM mode, the data is shifted into the shift register via any of the interfaces at the rate of 1-bit per command. After transmitting the last (9th) bit and exiting the MM mode, the interface is again in the normal mode and all other commands can be sent. Care should be taken that 9 bits of data (or a multiple of 9) are always transferred before exiting the MM mode, otherwise the bits will be in the wrong positions.

The value of the seal bit in the shift register is always zero at reset (also applies to all other bits). To make sure the security feature works correctly, the MM command is disabled until a refresh has been made. Once a refresh is completed, the seal bit value in the shift register is valid and permission to enter MM mode can thus be determined.

The 9 bits are shifted into the shift register in a predefined order: first 5 bits of $V_{CAL}[4:0]$, followed by 3 bits for $MF[2:0]$ and then the seal bit. The MSB is always first, that is the first bit shifted is $V_{CAL}[4]$ and the seal bit is the last bit.

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17.5 Interface commands

Instructions additional to those of the instruction set (Table 5) are given in Table 21.

Table 21 Additional instructions

| INSTRUCTION | D/C | R/W | COMMAND BYTE | | | | | | | | ACTION |
|---------------|-----|-----|--------------|----|----|----|----|----|----|----|--|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Reset | | | | | | | | | | | enable OTP circuitry |
| Function set | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | exit Power-down |
| REF (refresh) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | PC | switch HVgen on/off to force refresh of shift register |
| | | | | | | | | | | | wait 5 ms for refresh to take effect |
| Function set | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | set PD = 1 and H = 1 |
| MM | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | enter MM mode |

17.5.1 DISABLE OTP COMMAND

This is a special instruction for the PCF8813 which disables all included OTP circuitry. In this case, all OTP-related commands are inactive. V_{CAL} and MF have no effect on V_{LCD} and manufacture identification respectively. Once disabled, the mode can only be enabled via a reset.

17.5.2 MODULE MAKER CALIBRATION

Instruction (MM) enters the device into the calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set, then this mode cannot be accessed and the instruction will be ignored. Once in calibration mode all commands are interpreted as shift register data. The mode can only be exited by sending data with bit D7 set to logic 0. Reset will also clear this mode. Each shift register data byte is preceded by D/C = 0 and has only three significant bits, thus the remaining five bits are ignored. Bit D7 is the continuation bit (D7 = 1 indicates remain in MM mode; D7 = 0 indicates exit MM mode). D6 has to be logic 0 until the last bit when the seal bit is set, in which case this is set to logic 1 (D6 is set to logic 1 only when the high voltage used for programming the cells is about to be applied). Bit D0 is the data bit and its value is shifted into the OTP shift register on the falling edge of the SCLK clock.

17.5.3 REFRESH

The action of the refresh instruction (REF) is to force the OTP shift register to re-load from the non-volatile OTP cells. This instruction takes up to 5 ms to complete. During this time all other instructions may be sent.

In the PCF8813, the refresh instruction is associated with the power control instruction so that the shift register is refreshed automatically every time the high voltage generator is enabled or disabled. However, if this instruction is sent while in Power-down, the PC bits are updated but the refreshing is ignored.

17.6 Filling the shift register

An example of the sequence of commands and data for filling the shift register is shown in Table 22. This example uses the values V_{CAL} = -4 (11100B), MF = 4 (100B is the Philips identifying code) and the seal bit is 0.

It is assumed that the PCF8813 has just been reset. After transmitting the last bit the PCF8813 can exit or remain in MM mode (see Table 22, step 1). When in MM mode, the interface does not recognize commands in the normal sense.

After this sequence has been applied, it is possible to observe the impact of the data shifted in. The sequence described is not useful for OTP programming because the number of bits with value = 1 is greater than that allowed for programming (see Section 17.7). Figure 49 shows the shift register after this action.

(67 + 1) × 102 pixels matrix LCD driver

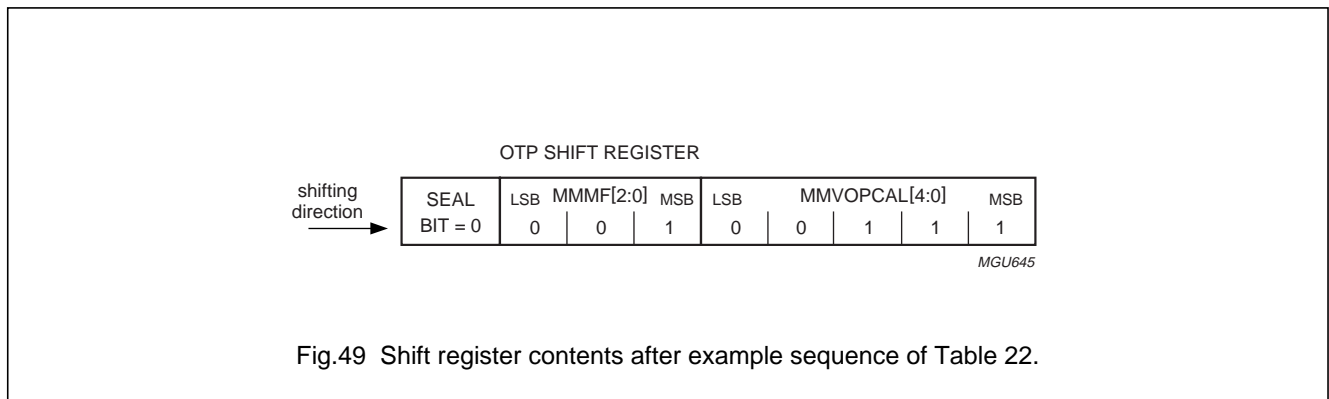
PCF8813

Table 22 Example sequence of shift register filling

| STEP | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACTION |
|------|-------|-----|----|----|----|----|----|----|----|----|---|
| 1 | reset | | | | | | | | | | reset to enable OTP circuitry |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | exit Power-down (PD = 0) |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | PC | switch HV/gen on/off to force refresh of shift register |
| | | | | | | | | | | | wait 5 ms for refresh to take effect |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | set PD to 1 ⁽²⁾ and H to 1 |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | enter MM mode |
| 6 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | shift-in data; V _{CAL} [4] is first bit ⁽³⁾ |
| 7 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | V _{CAL} [3] |
| 8 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | V _{CAL} [2] |
| 9 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | V _{CAL} [1] |
| 10 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | V _{CAL} [0] |
| 11 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | MF[2] |
| 12 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | MF[1] |
| 13 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | MF[0] |
| 14 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | seal bit; remain in MM mode |

Notes

1. X = don't care.
2. PD does not have to be set to 1 if the effects of V_{CAL} are intended to be observed on V_{LCDOUT}.
3. Bit data is not in the correct shift register position until all bits have been sent.



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17.7 Programming flow

Programming is achieved in MM mode and with application of the programming voltages. Since the data for programming the OTP cell is contained in the corresponding shift register cell, the shift register cell must be loaded with a 1 in order to program the corresponding OTP cell. If the shift register cell contains a 0, then no action will take place when the programming voltages are applied.

Once programmed, an OTP cell cannot be de-programmed. Also, a previously programmed cell that is an OTP cell containing a 1 must not be re-programmed.

During programming a substantial current flows in the V_{LCDIN} pad. For this reason programming only one OTP

cell at a time is recommended. This is achieved by filling all but one shift register cells with 0.

The programming specification refers to the voltages at the chip pads, therefore contact resistance must be considered by the user.

An example of the sequence of commands and data for OTP programming is given in Table 23. The order for programming cells is not significant but it is recommended that the seal bit is programmed last. Once the seal bit has been programmed it is not possible to re-enter the MM mode.

It is assumed that the PCF8813 has been reset just before the programming commences.

Table 23 Example sequence for OTP programming

| STEP | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACTION |
|---|-----|-----|-------|----|----|----|----|----|----|----|---|
| 1 | | | reset | | | | | | | | enable OTP by applying a reset |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | exit Power-down (PD = 0) |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | PC | switch HVgen on/off to force refresh of shift register |
| | | | | | | | | | | | wait 5 ms for refresh to take effect |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | re-enter Power-down (PD = 1 and H = 1) |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | enter MM mode |
| 6 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | $V_{CAL}[4]$ (the only bit with value of 1) |
| 7 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | $V_{CAL}[3]$ |
| 8 | 0 | 0 | 1 | 0 | X | X | X | X | X | 1 | $V_{CAL}[2]$ |
| 9 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | $V_{CAL}[1]$ |
| 10 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | $V_{CAL}[0]$ |
| 11 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | MF[2] |
| 12 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | MF[1] |
| 13 | 0 | 0 | 1 | 0 | X | X | X | X | X | 0 | MF[0] |
| 14 | 0 | 0 | 1 | 1 | X | X | X | X | X | 0 | seal bit; remain in CALMM mode |
| 15 | – | – | – | – | – | – | – | – | – | – | apply programming voltage at pads $V_{OTPPROG}$ and V_{LCDIN} |
| Repeat steps 6 to 15 for each bit that should be programmed to 1 | | | | | | | | | | | |
| 15 | – | – | – | – | – | – | – | – | – | – | apply external reset |

Note

1. X = don't care.

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17.8 Programming specification

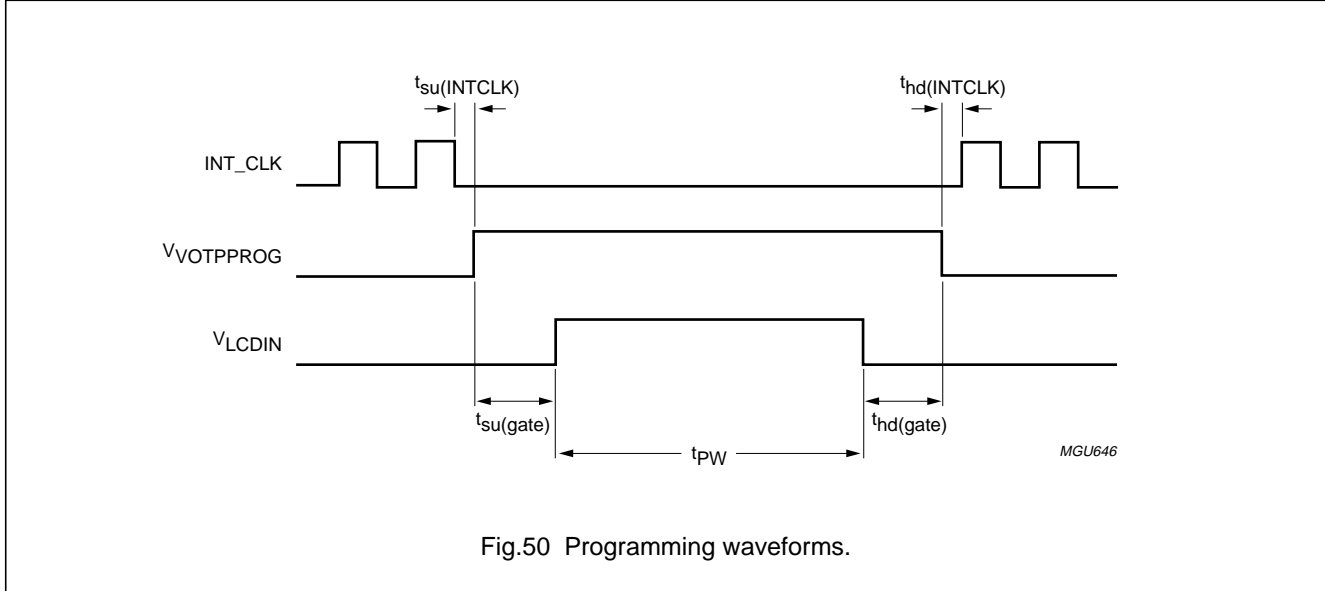


Fig.50 Programming waveforms.

Table 24 Programming parameters

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------------|---|--|-----------|-----------|--------------------------|--------|
| V _{DD1} | logic supply voltage | | 2.4 | – | 3.3 | V |
| V _{OTPPROG} | voltage applied to pad V _{OTPPROG} | V _{OTPPROG} relative to V _{SS1} ; note 1 programming active programming inactive | 11.0 0 | 11.5 – | 12.0 V _{DD1} | V V |
| V _{LCDIN} | voltage applied to pad V _{LCDIN} | V _{LCDIN} relative to V _{SS1} ; notes 1, 2 programming active programming inactive | 9.0 0 | 9.50 – | 10.5 V _{DD2} | V V |
| I _{OTPPROG} | current drawn during programming | | – | 100 | 200 | μA |
| I _{LCDIN} | current drawn during programming | when programming one bit to logic 1 | – | 850 | 1000 | μA |
| T _{prog} | ambient temperature during programming | | 0 | 25 | 40 | °C |
| t _{su} (INTCLK) | internal data set-up time after last clock | | 1 | – | – | μs |
| t _{hd} (INTCLK) | internal data hold time before next clock | | 1 | – | – | μs |
| t _{su} (gate) | V _{OTPPROG} set-up time prior to programming | | 1 | – | 10 | ms |
| t _{hd} (gate) | V _{OTPPROG} hold time after programming | | 1 | – | 10 | ms |
| t _{pW} | programming voltage pulse width | | 100 | 120 | 200 | ms |

Notes

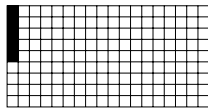
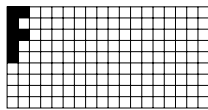
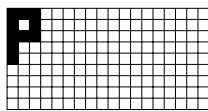
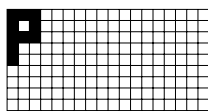
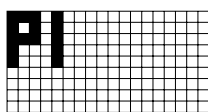
1. The voltage drop across the ITO track and zebra connector must be taken into account to guarantee sufficient voltage at the chip pads.
2. The high voltage generator must be disabled (V_{PR} = 0 and PRS = 0) when pad V_{LCDIN} is being driven.

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17.9 Programming examples

Table 25 Programming example for PCF8813 with serial interface (3-line serial, 3-line SPI or 4-line SPI)

| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|--|--|
| | D/C | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 1 | start | | | | | | | | | | SC \bar{E} is going low |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | function set: PD = 0, V = 0; select extended instruction set (H = 1) |
| 3 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | set PRS to higher programming range (PRS = 1) |
| 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | set V _{PR} : V _{PR} * = (a + 132* × b) = 8.596 V (required voltage is dependent on liquid crystal operating environment) |
| 5 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | function set: PD = 0, V = 0; select normal instruction set (H = 0) |
| 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | display control: set normal mode (D = 1 and E = 0) |
| 7 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | | set data order: DO = 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 8 | – | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | | option available in 3-line SPI for setting display data length command (7 shown) |
| | – | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| 9 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  | data write: Y and X are initialized to 0 by default, so they are not set here |
| 10 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  | data write |
| 11 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  | data write |
| 12 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | data write |
| 13 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  | data write |

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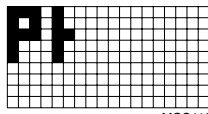
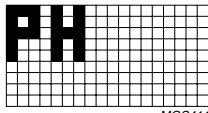

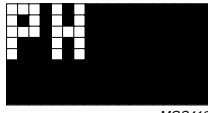

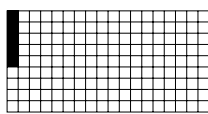
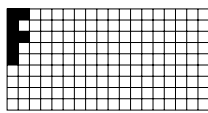
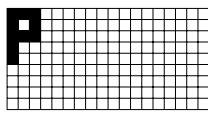
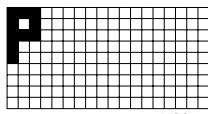
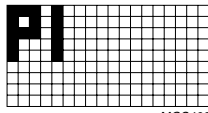
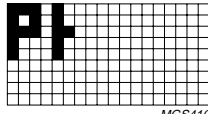
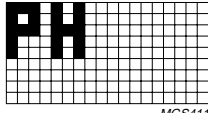
| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|--|---|
| | D/C | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 14 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  | data write |
| 15 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  | data write |
| 16 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  | display control: set inverse video mode (D = 1 and E = 1) |
| 17 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | set X address of RAM: set address to '0000000' |
| 18 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | data write |

Table 26 Programming example for PCF8813 with I²C -bus

| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|------|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|---------|--|
| | D/C | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 1 | I ² C-bus start | | | | | | | | | | |
| 2 | – | 0 | 1 | 1 | 1 | 1 | SA1 | SA0 | 0 | | slave address for write |
| 3 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with cleared CO bit and D/C set to logic 0 |
| 4 | – | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | function set: PD = 0, V = 0; select extended instruction set (H = 1) |
| 5 | – | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | set PRS to higher programming range (PRS = 1) |
| 6 | – | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | set V _{PR} : V _{PR} * = (a + 132* × b) = 8.596 V (required voltage is dependent on liquid crystal operating environment) |
| 7 | – | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | function set: PD = 0; V = 0; select normal instruction set (H = 0) |

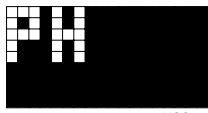
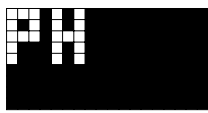
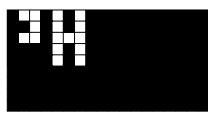
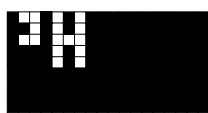

(67 + 1) × 102 pixels matrix LCD driver

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| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION | |
|------|----------------------------|----------------------------|-----|-----|-----|-----|-----|-----|-----|---|---|---|
| | D/C | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| 8 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | display control: set normal mode (D = 1 and E = 0) | |
| 9 | – | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | | display configuration (DO = 0) | |
| | – | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | |
| 10 | – | I ² C-bus start | | | | | | | | | | restart: to write into the display RAM the D/C must be set to logic 1, therefore a control byte is needed |
| 11 | – | 0 | 1 | 1 | 1 | 1 | SA1 | SA0 | 0 | | slave address for write | |
| 12 | – | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with cleared CO bit and D/C set to logic 1 | |
| 13 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | – |  <small>MGS405</small> | data write: Y and X are initialized to 0 by default, so they are not set here | |
| 14 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | – |  <small>MGS406</small> | data write | |
| 15 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | – |  <small>MGS407</small> | data write | |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | – |  <small>MGS407</small> | data write | |
| 17 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | – |  <small>MGS409</small> | data write | |
| 18 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | – |  <small>MGS410</small> | data write | |
| 19 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | – |  <small>MGS411</small> | data write | |
| 20 | I ² C-bus start | | | | | | | | | | restart | |
| 21 | – | 0 | 1 | 1 | 1 | 1 | SA1 | SA0 | 0 | | slave address for write | |
| 22 | – | 1 | | | | | | | | | control byte with set CO bit and D/C set to logic 0 | |

$(67 + 1) \times 102$ pixels matrix LCD driver

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| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|------|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|--|---|
| | D/C | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 23 | – | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  | display control: set inverse video mode (D = 1 and E = 1) |
| 24 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with set CO bit and D/C set to logic 0 |
| 25 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | Set X address of RAM: set address to 0000000 |
| 26 | – | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with set CO bit and D/C set to logic 1 |
| 27 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | data write |
| 28 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with set CO bit and D/C set to logic 0 |
| 29 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | set X address of RAM: set address to 0000000 |
| 30 | I ² C-bus start | | | | | | | | | | restart |
| 31 | – | 0 | 1 | 1 | 1 | 1 | SA1 | SA0 | 0 | | slave address for write |
| 32 | – | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with set CO bit and D/C set to logic 1 |
| 33 | – | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |  | write data |
| 34 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte with set CO bit and D/C set to logic 0 |

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18 APPLICATION INFORMATION

For additional application information, refer to application note "AN10170".

18.1 Protection from light

Semiconductors are light-sensitive. Exposure to light sources can cause malfunctions, therefore the IC should be protected from light in the application. Light protection needs to be applied to all sides of the IC (front, rear and all edges).

18.2 Application examples

In the following application examples, the required minimum values of the external capacitors are:

- C_{VLCD} = 100 nF minimum
- C_{VDD}, C_{VDD1} and C_{VDD2} = 1 μF minimum
- Higher capacitor values are recommended for ripple reduction.

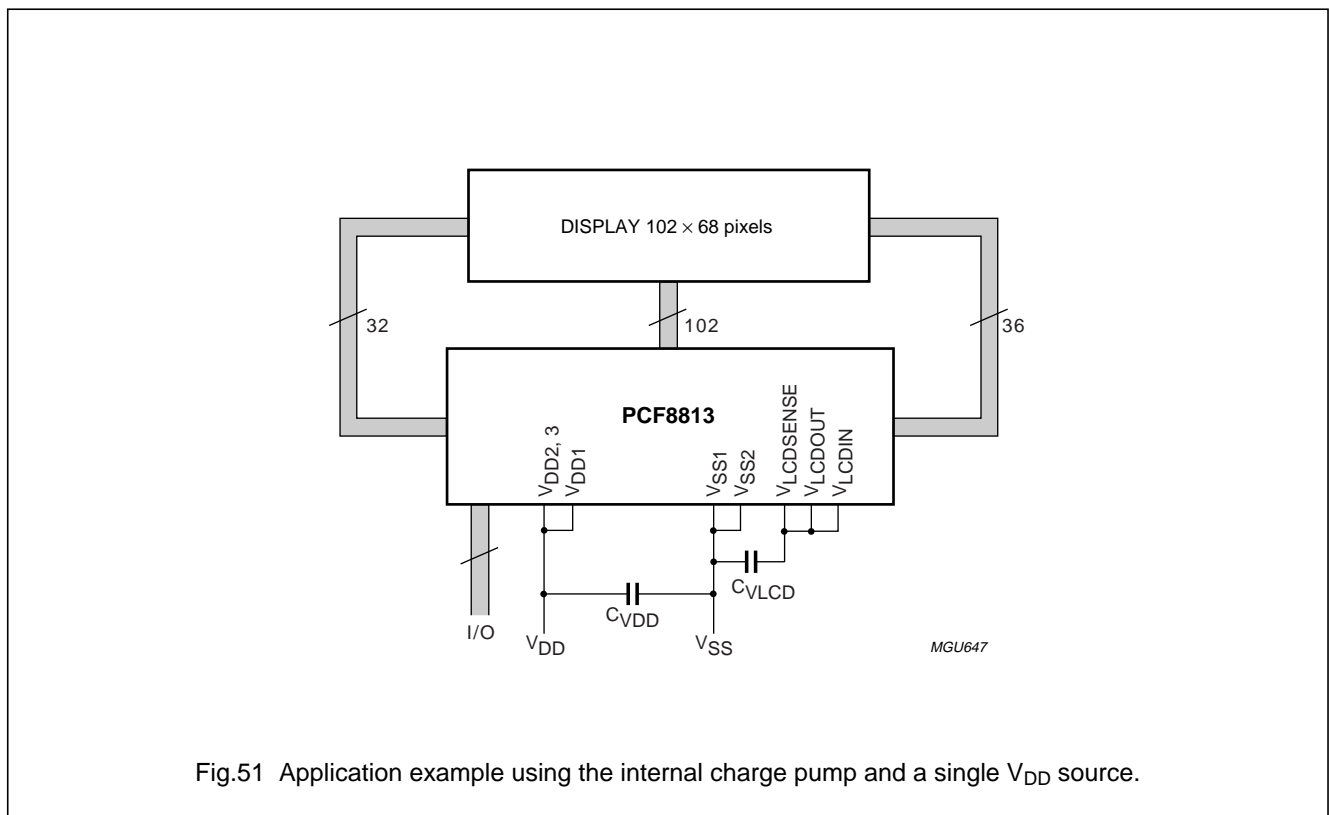
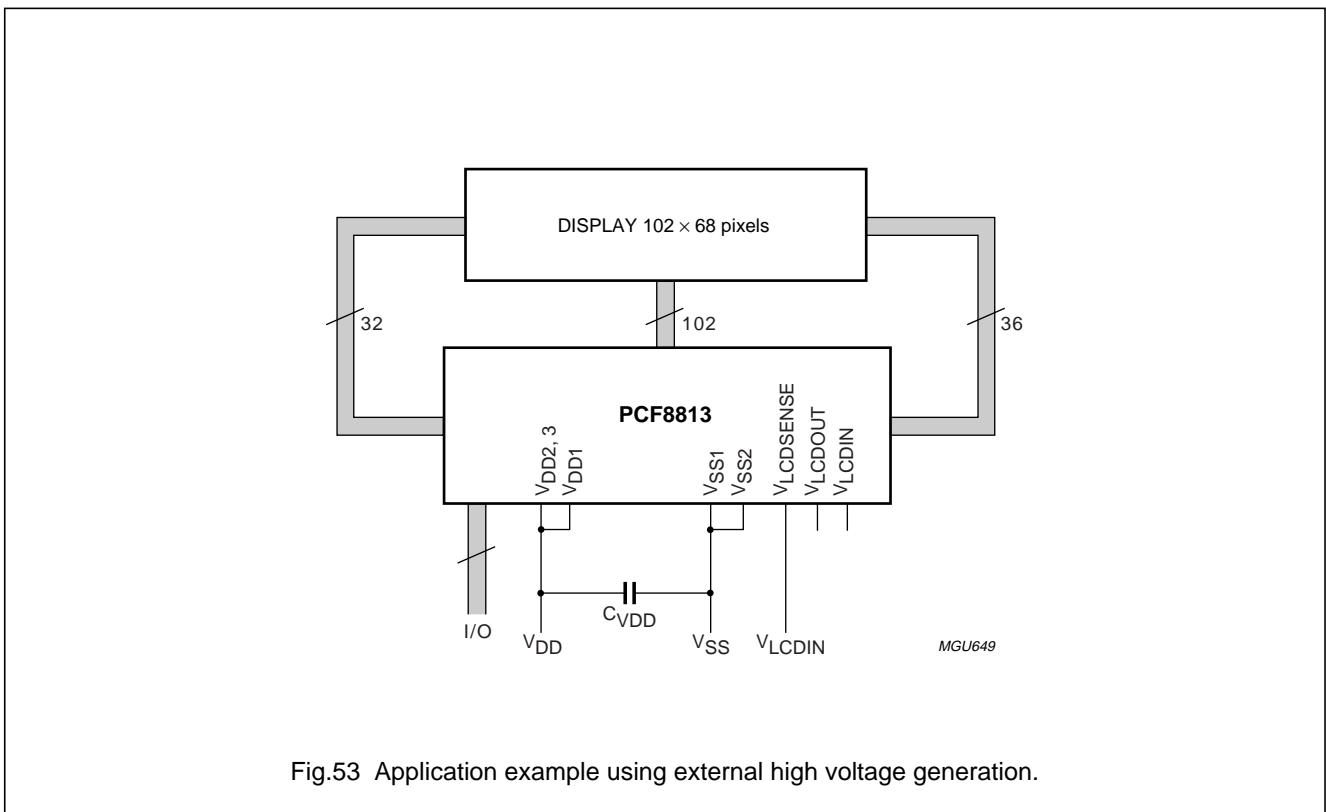
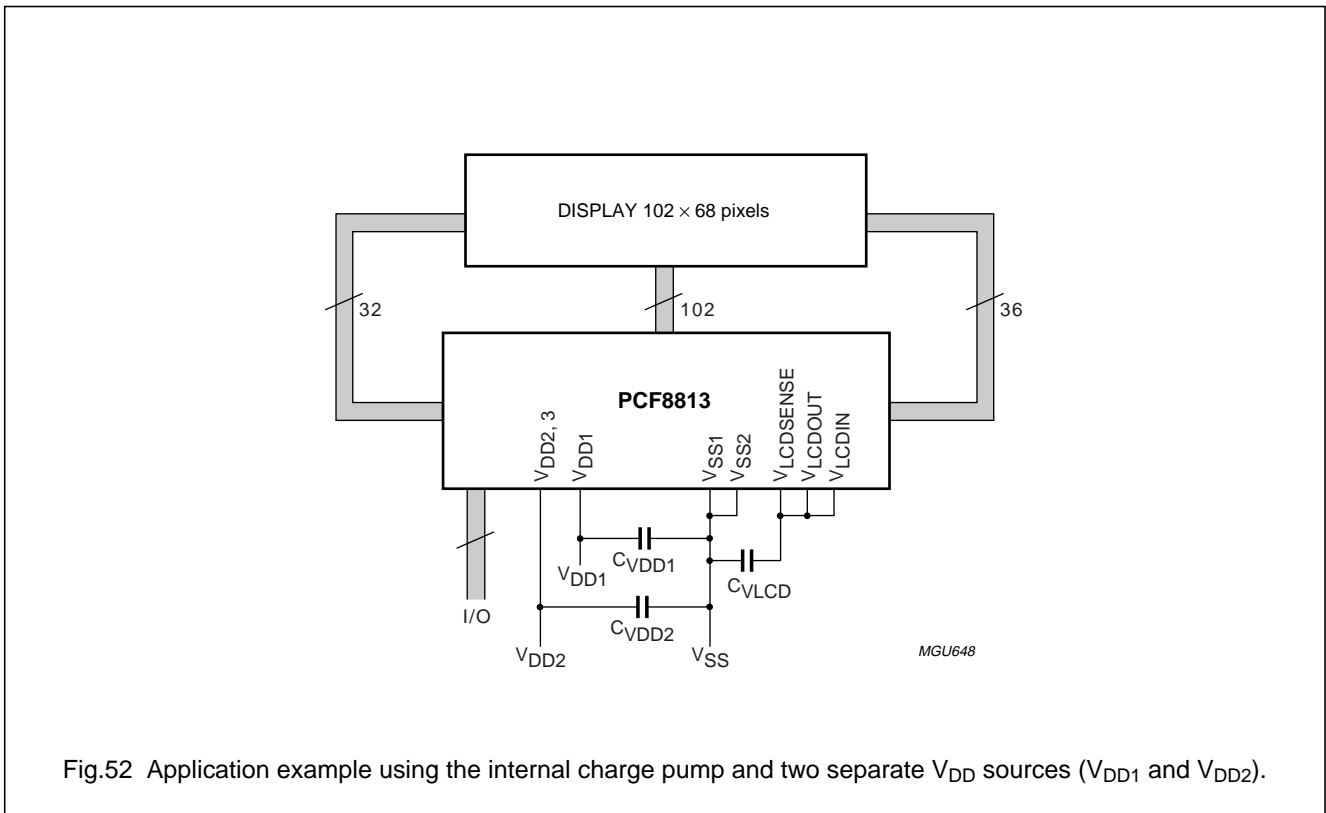


Fig.51 Application example using the internal charge pump and a single V_{DD} source.

(67 + 1) × 102 pixels matrix LCD driver

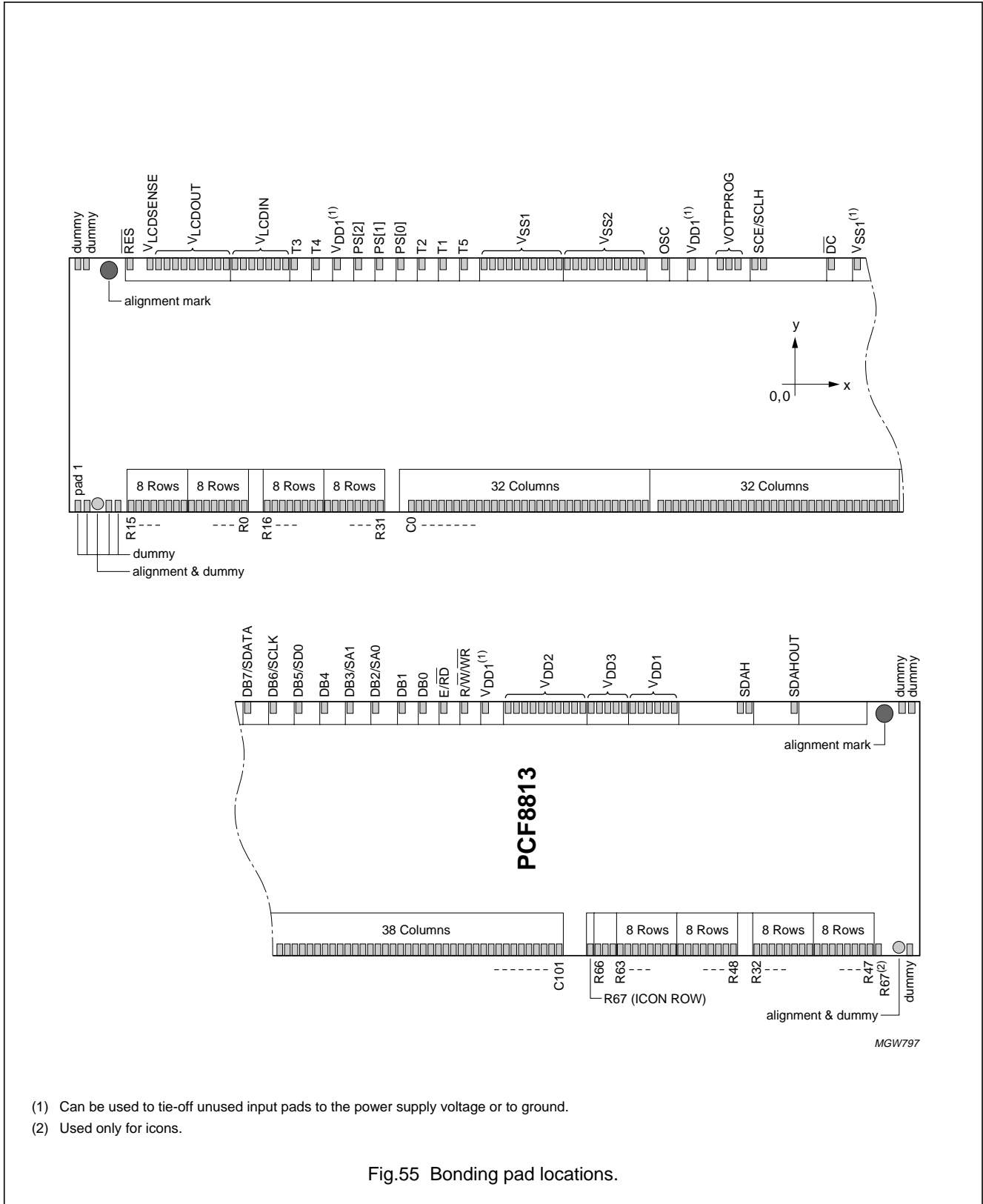
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(67 + 1) × 102 pixels matrix LCD driver

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20 BONDING PAD INFORMATION



- (1) Can be used to tie-off unused input pads to the power supply voltage or to ground.
- (2) Used only for icons.

Fig.55 Bonding pad locations.

$(67 + 1) \times 102$ pixels matrix LCD driver

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Table 27 Bonding pad locations

All x and y coordinates are referenced to the centre of the chip; dummy bumps should never be connected to any electrical nodes; dimensions in μm ; see Fig.55.

| SYMBOL | PAD | COORDINATES | |
|---------------------|-----|-------------|--------|
| | | x | y |
| dummy | 1 | -5328 | +814.5 |
| dummy | 2 | -5328 | -814.5 |
| dummy | 3 | -5274 | -814.5 |
| dummy and alignment | 4 | -5175 | -814.5 |
| dummy | 5 | -5085 | -814.5 |
| dummy | 6 | -5031 | -814.5 |
| R15 | 7 | -4869 | -814.5 |
| R14 | 8 | -4815 | -814.5 |
| R13 | 9 | -4761 | -814.5 |
| R12 | 10 | -4707 | -814.5 |
| R11 | 11 | -4653 | -814.5 |
| R10 | 12 | -4599 | -814.5 |
| R9 | 13 | -4545 | -814.5 |
| R8 | 14 | -4491 | -814.5 |
| R7 | 15 | -4437 | -814.5 |
| R6 | 16 | -4383 | -814.5 |
| R5 | 17 | -4329 | -814.5 |
| R4 | 18 | -4275 | -814.5 |
| R3 | 19 | -4221 | -814.5 |
| R2 | 20 | -4167 | -814.5 |
| R1 | 21 | -4113 | -814.5 |
| R0 | 22 | -4059 | -814.5 |
| R16 | 23 | -3843 | -814.5 |
| R17 | 24 | -3789 | -814.5 |
| R18 | 25 | -3735 | -814.5 |
| R19 | 26 | -3681 | -814.5 |
| R20 | 27 | -3627 | -814.5 |
| R21 | 28 | -3573 | -814.5 |
| R22 | 29 | -3519 | -814.5 |
| R23 | 30 | -3465 | -814.5 |
| R24 | 31 | -3411 | -814.5 |
| R25 | 32 | -3357 | -814.5 |
| R26 | 33 | -3303 | -814.5 |
| R27 | 34 | -3249 | -814.5 |
| R28 | 35 | -3195 | -814.5 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|--------|
| | | x | y |
| R29 | 36 | -3141 | -814.5 |
| R30 | 37 | -3087 | -814.5 |
| R31 | 38 | -3033 | -814.5 |
| C0 | 39 | -2871 | -814.5 |
| C1 | 40 | -2817 | -814.5 |
| C2 | 41 | -2763 | -814.5 |
| C3 | 42 | -2709 | -814.5 |
| C4 | 43 | -2655 | -814.5 |
| C5 | 44 | -2601 | -814.5 |
| C6 | 45 | -2547 | -814.5 |
| C7 | 46 | -2493 | -814.5 |
| C8 | 47 | -2439 | -814.5 |
| C9 | 48 | -2385 | -814.5 |
| C10 | 49 | -2331 | -814.5 |
| C11 | 50 | -2277 | -814.5 |
| C12 | 51 | -2223 | -814.5 |
| C13 | 52 | -2169 | -814.5 |
| C14 | 53 | -2115 | -814.5 |
| C15 | 54 | -2061 | -814.5 |
| C16 | 55 | -2007 | -814.5 |
| C17 | 56 | -1953 | -814.5 |
| C18 | 57 | -1899 | -814.5 |
| C19 | 58 | -1845 | -814.5 |
| C20 | 59 | -1791 | -814.5 |
| C21 | 60 | -1737 | -814.5 |
| C22 | 61 | -1683 | -814.5 |
| C23 | 62 | -1629 | -814.5 |
| C24 | 63 | -1575 | -814.5 |
| C25 | 64 | -1521 | -814.5 |
| C26 | 65 | -1467 | -814.5 |
| C27 | 66 | -1413 | -814.5 |
| C28 | 67 | -1359 | -814.5 |
| C29 | 68 | -1305 | -814.5 |
| C30 | 69 | -1251 | -814.5 |
| C31 | 70 | -1197 | -814.5 |
| C32 | 71 | -1035 | -814.5 |
| C33 | 72 | -981 | -814.5 |
| C34 | 73 | -927 | -814.5 |
| C35 | 74 | -873 | -814.5 |

$(67 + 1) \times 102$ pixels matrix LCD driver

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|--------|
| | | x | y |
| C36 | 75 | -819 | -814.5 |
| C37 | 76 | -765 | -814.5 |
| C38 | 77 | -711 | -814.5 |
| C39 | 78 | -657 | -814.5 |
| C40 | 79 | -603 | -814.5 |
| C41 | 80 | -549 | -814.5 |
| C42 | 81 | -495 | -814.5 |
| C43 | 82 | -441 | -814.5 |
| C44 | 83 | -387 | -814.5 |
| C45 | 84 | -333 | -814.5 |
| C46 | 85 | -279 | -814.5 |
| C47 | 86 | -225 | -814.5 |
| C48 | 87 | -171 | -814.5 |
| C49 | 88 | -117 | -814.5 |
| C50 | 89 | -63 | -814.5 |
| C51 | 90 | -9 | -814.5 |
| C52 | 91 | +45 | -814.5 |
| C53 | 92 | +99 | -814.5 |
| C54 | 93 | +153 | -814.5 |
| C55 | 94 | +207 | -814.5 |
| C56 | 95 | +261 | -814.5 |
| C57 | 96 | +315 | -814.5 |
| C58 | 97 | +369 | -814.5 |
| C59 | 98 | +423 | -814.5 |
| C60 | 99 | +477 | -814.5 |
| C61 | 100 | +531 | -814.5 |
| C62 | 101 | +585 | -814.5 |
| C63 | 102 | +639 | -814.5 |
| C64 | 103 | +801 | -814.5 |
| C65 | 104 | +855 | -814.5 |
| C66 | 105 | +909 | -814.5 |
| C67 | 106 | +963 | -814.5 |
| C68 | 107 | +1017 | -814.5 |
| C69 | 108 | +1071 | -814.5 |
| C70 | 109 | +1125 | -814.5 |
| C71 | 110 | +1179 | -814.5 |
| C72 | 111 | +1233 | -814.5 |
| C73 | 112 | +1287 | -814.5 |
| C74 | 113 | +1341 | -814.5 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|--------|
| | | x | y |
| C75 | 114 | +1395 | -814.5 |
| C76 | 115 | +1449 | -814.5 |
| C77 | 116 | +1503 | -814.5 |
| C78 | 117 | +1557 | -814.5 |
| C79 | 118 | +1611 | -814.5 |
| C80 | 119 | +1665 | -814.5 |
| C81 | 120 | +1719 | -814.5 |
| C82 | 121 | +1773 | -814.5 |
| C83 | 122 | +1827 | -814.5 |
| C84 | 123 | +1881 | -814.5 |
| C85 | 124 | +1935 | -814.5 |
| C86 | 125 | +1989 | -814.5 |
| C87 | 126 | +2043 | -814.5 |
| C88 | 127 | +2097 | -814.5 |
| C89 | 128 | +2151 | -814.5 |
| C90 | 129 | +2205 | -814.5 |
| C91 | 130 | +2259 | -814.5 |
| C92 | 131 | +2313 | -814.5 |
| C93 | 132 | +2367 | -814.5 |
| C94 | 133 | +2421 | -814.5 |
| C95 | 134 | +2475 | -814.5 |
| C96 | 135 | +2529 | -814.5 |
| C97 | 136 | +2583 | -814.5 |
| C98 | 137 | +2637 | -814.5 |
| C99 | 138 | +2691 | -814.5 |
| C100 | 139 | +2745 | -814.5 |
| C101 | 140 | +2799 | -814.5 |
| R67 | 141 | +2961 | -814.5 |
| R66 | 142 | +3015 | -814.5 |
| R65 | 143 | +3069 | -814.5 |
| R64 | 144 | +3123 | -814.5 |
| R63 | 145 | +3177 | -814.5 |
| R62 | 146 | +3231 | -814.5 |
| R61 | 147 | +3285 | -814.5 |
| R60 | 148 | +3339 | -814.5 |
| R59 | 149 | +3393 | -814.5 |
| R58 | 150 | +3447 | -814.5 |
| R57 | 151 | +3501 | -814.5 |
| R56 | 152 | +3555 | -814.5 |

$(67 + 1) \times 102$ pixels matrix LCD driver

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| SYMBOL | PAD | COORDINATES | |
|---------------------|-----|-------------|--------|
| | | x | y |
| R55 | 153 | +3609 | -814.5 |
| R54 | 154 | +3663 | -814.5 |
| R53 | 155 | +3717 | -814.5 |
| R52 | 156 | +3771 | -814.5 |
| R51 | 157 | +3825 | -814.5 |
| R50 | 158 | +3879 | -814.5 |
| R49 | 159 | +3933 | -814.5 |
| R48 | 160 | +3987 | -814.5 |
| R32 | 161 | +4203 | -814.5 |
| R33 | 162 | +4257 | -814.5 |
| R34 | 163 | +4311 | -814.5 |
| R35 | 164 | +4365 | -814.5 |
| R36 | 165 | +4419 | -814.5 |
| R37 | 166 | +4473 | -814.5 |
| R38 | 167 | +4527 | -814.5 |
| R39 | 168 | +4581 | -814.5 |
| R40 | 169 | +4635 | -814.5 |
| R41 | 170 | +4689 | -814.5 |
| R42 | 171 | +4743 | -814.5 |
| R43 | 172 | +4797 | -814.5 |
| R44 | 173 | +4851 | -814.5 |
| R45 | 174 | +4905 | -814.5 |
| R46 | 175 | +4959 | -814.5 |
| R47 | 176 | +5013 | -814.5 |
| R67 | 177 | +5067 | -814.5 |
| dummy and alignment | 178 | +5229 | -814.5 |
| dummy | 179 | +5328 | -814.5 |
| dummy | 180 | +5328 | +814.5 |
| dummy | 181 | +5274 | +814.5 |
| dummy | 182 | +4752 | +814.5 |
| SDAHOUT | 183 | +4500 | +814.5 |
| SDAH | 184 | +4122 | +814.5 |
| SDAH | 185 | +4068 | +814.5 |
| V _{DD1} | 186 | +3528 | +814.5 |
| V _{DD1} | 187 | +3474 | +814.5 |
| V _{DD1} | 188 | +3420 | +814.5 |
| V _{DD1} | 189 | +3366 | +814.5 |
| V _{DD1} | 190 | +3312 | +814.5 |
| V _{DD1} | 191 | +3258 | +814.5 |

| SYMBOL | PAD | COORDINATES | |
|----------------------|-----|-------------|--------|
| | | x | y |
| V _{DD3} | 192 | +3204 | +814.5 |
| V _{DD3} | 193 | +3150 | +814.5 |
| V _{DD3} | 194 | +3096 | +814.5 |
| V _{DD3} | 195 | +3042 | +814.5 |
| V _{DD3} | 196 | +2988 | +814.5 |
| V _{DD2} | 197 | +2934 | +814.5 |
| V _{DD2} | 198 | +2880 | +814.5 |
| V _{DD2} | 199 | +2826 | +814.5 |
| V _{DD2} | 200 | +2772 | +814.5 |
| V _{DD2} | 201 | +2718 | +814.5 |
| V _{DD2} | 202 | +2664 | +814.5 |
| V _{DD2} | 203 | +2610 | +814.5 |
| V _{DD2} | 204 | +2556 | +814.5 |
| V _{DD2} | 205 | +2502 | +814.5 |
| V _{DD2} | 206 | +2448 | +814.5 |
| V _{DD1} | 207 | +2286 | +814.5 |
| R/W/WR | 208 | +2124 | +814.5 |
| E/RD | 209 | +1962 | +814.5 |
| DB0 | 210 | +1746 | +814.5 |
| DB1 | 211 | +1530 | +814.5 |
| DB2/SA0 | 212 | +1314 | +814.5 |
| DB3/SA1 | 213 | +1098 | +814.5 |
| DB4 | 214 | +882 | +814.5 |
| DB5/SDOUT | 215 | +666 | +814.5 |
| DB6/ SCLK | 216 | +450 | +814.5 |
| DB7/SDATA | 217 | +234 | +814.5 |
| V _{SS1} | 218 | +72 | +814.5 |
| D/C | 219 | -90 | +814.5 |
| SCE/SCLH | 220 | -630 | +814.5 |
| SCE/SCLH | 221 | -684 | +814.5 |
| V _{OTPPROG} | 222 | -792 | +814.5 |
| V _{OTPPROG} | 223 | -846 | +814.5 |
| V _{OTPPROG} | 224 | -900 | +814.5 |
| V _{DD1} | 225 | -1008 | +814.5 |
| OSC | 226 | -1296 | +814.5 |
| V _{SS2} | 227 | -1458 | +814.5 |
| V _{SS2} | 228 | -1512 | +814.5 |
| V _{SS2} | 229 | -1566 | +814.5 |
| V _{SS2} | 230 | -1620 | +814.5 |

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| SYMBOL | PAD | COORDINATES | |
|------------------|-----|-------------|--------|
| | | x | y |
| V _{SS2} | 231 | -1674 | +814.5 |
| V _{SS2} | 232 | -1728 | +814.5 |
| V _{SS2} | 233 | -1782 | +814.5 |
| V _{SS2} | 234 | -1836 | +814.5 |
| V _{SS2} | 235 | -1890 | +814.5 |
| V _{SS2} | 236 | -1944 | +814.5 |
| V _{SS1} | 237 | -1998 | +814.5 |
| V _{SS1} | 238 | -2052 | +814.5 |
| V _{SS1} | 239 | -2106 | +814.5 |
| V _{SS1} | 240 | -2160 | +814.5 |
| V _{SS1} | 241 | -2214 | +814.5 |
| V _{SS1} | 242 | -2268 | +814.5 |
| V _{SS1} | 243 | -2322 | +814.5 |
| V _{SS1} | 244 | -2376 | +814.5 |
| V _{SS1} | 245 | -2430 | +814.5 |
| V _{SS1} | 246 | -2484 | +814.5 |
| T5 | 247 | -2646 | +814.5 |
| T1 | 248 | -2808 | +814.5 |
| T2 | 249 | -2970 | +814.5 |
| PS0 | 250 | -3132 | +814.5 |
| PS1 | 251 | -3294 | +814.5 |
| PS2 | 252 | -3456 | +814.5 |

| SYMBOL | PAD | COORDINATES | |
|-----------------------|-----|-------------|--------|
| | | x | y |
| V _{DD1} | 253 | -3618 | +814.5 |
| T4 | 254 | -3780 | +814.5 |
| T3 | 255 | -3942 | +814.5 |
| V _{LCDIN} | 256 | -3996 | +814.5 |
| V _{LCDIN} | 257 | -4050 | +814.5 |
| V _{LCDIN} | 258 | -4104 | +814.5 |
| V _{LCDIN} | 259 | -4158 | +814.5 |
| V _{LCDIN} | 260 | -4212 | +814.5 |
| V _{LCDIN} | 261 | -4266 | +814.5 |
| V _{LCDIN} | 262 | -4320 | +814.5 |
| V _{LCDOUT} | 263 | -4374 | +814.5 |
| V _{LCDOUT} | 264 | -4428 | +814.5 |
| V _{LCDOUT} | 265 | -4482 | +814.5 |
| V _{LCDOUT} | 266 | -4536 | +814.5 |
| V _{LCDOUT} | 267 | -4590 | +814.5 |
| V _{LCDOUT} | 268 | -4644 | +814.5 |
| V _{LCDOUT} | 269 | -4698 | +814.5 |
| V _{LCDOUT} | 270 | -4752 | +814.5 |
| V _{LCDOUT} | 271 | -4806 | +814.5 |
| V _{LCDSENSE} | 272 | -4860 | +814.5 |
| RES | 273 | -5076 | +814.5 |
| dummy | 274 | -5274 | +814.5 |

$(67 + 1) \times 102$ pixels matrix LCD driver

PCF8813

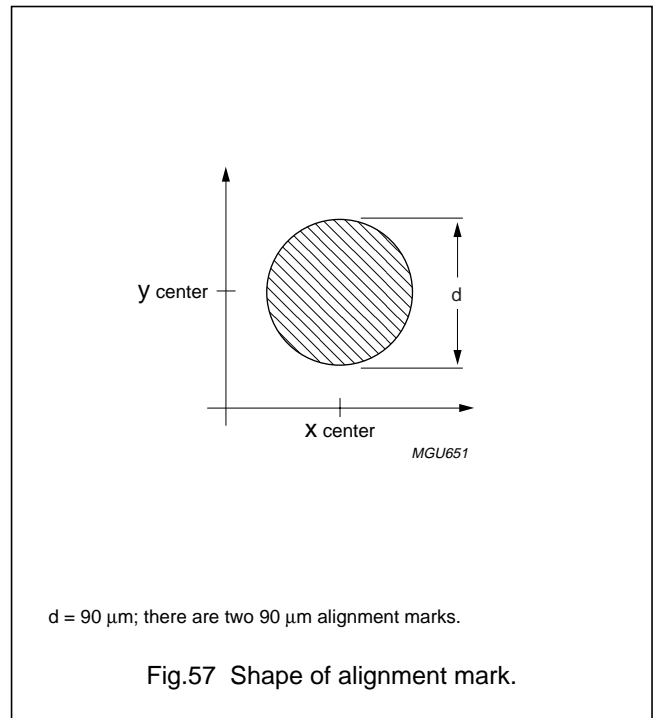
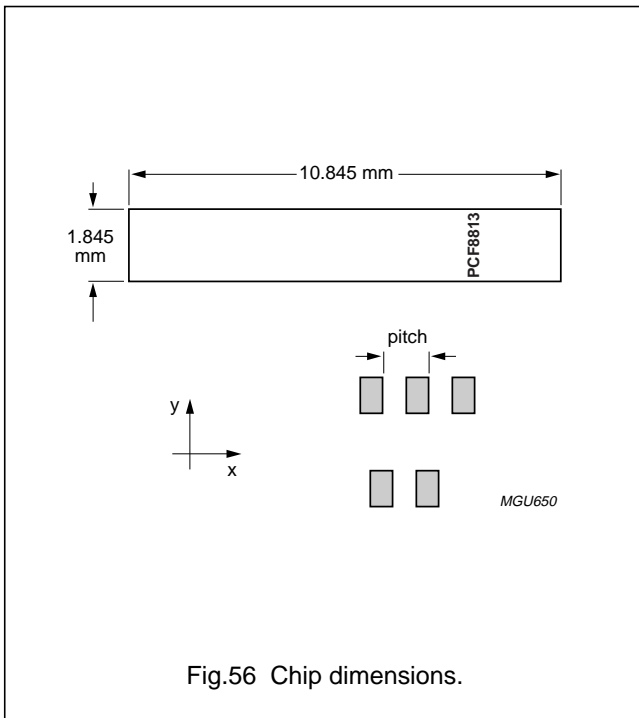


Table 28 Bump size

| PARAMETER | VALUE (μm) |
|--|----------------------------|
| Bump width | 32 |
| Bump length | 81 |
| Bump height | 17.5 |
| Minimum pad pitch | 54 |
| Pad size, aluminium | 45×81 |
| Maximum wafer thickness, including bumps | 430 |
| Typical wafer thickness, without bumps | 381 |

(67 + 1) × 102 pixels matrix LCD driver

PCF8813

21 TRAY INFORMATION

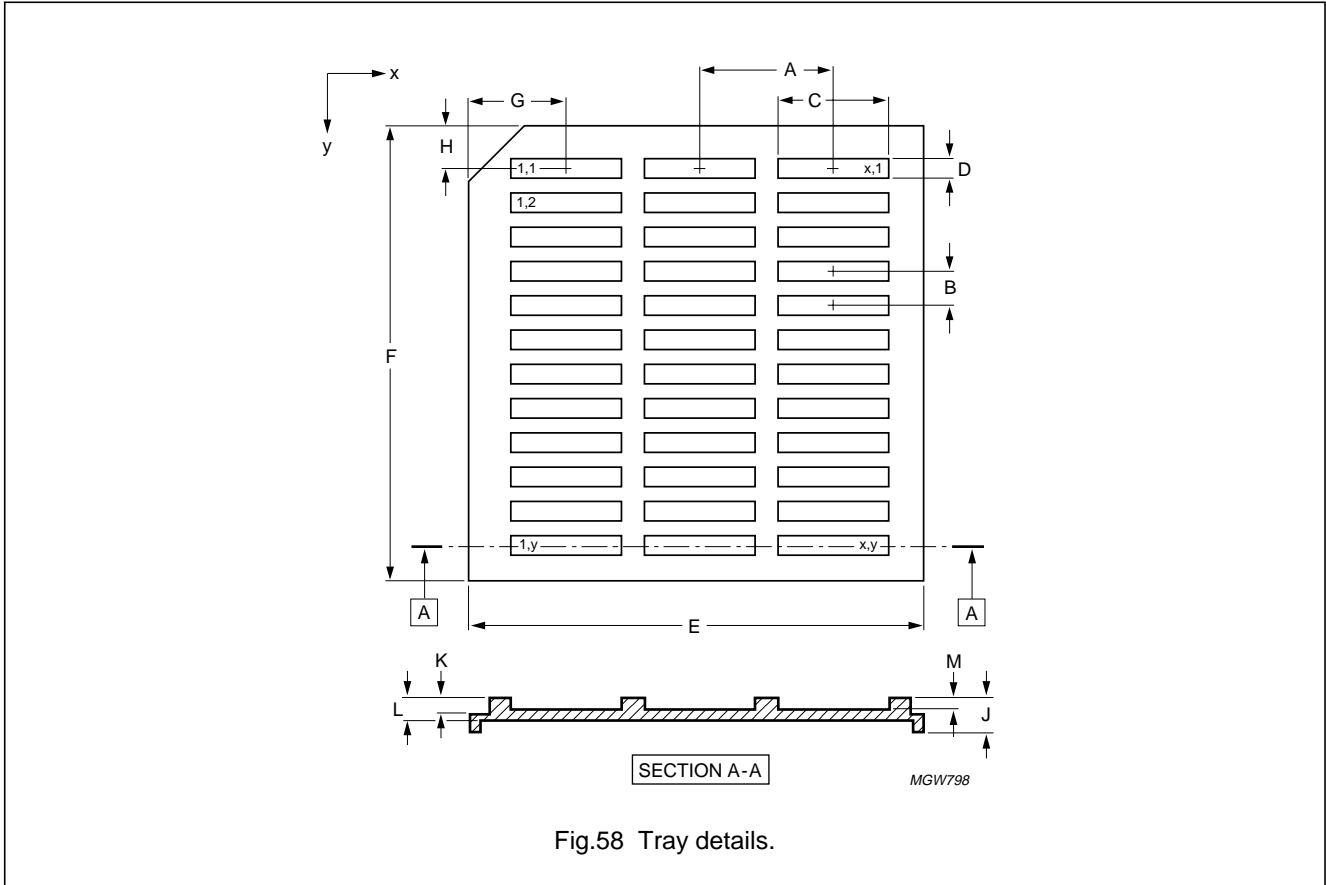
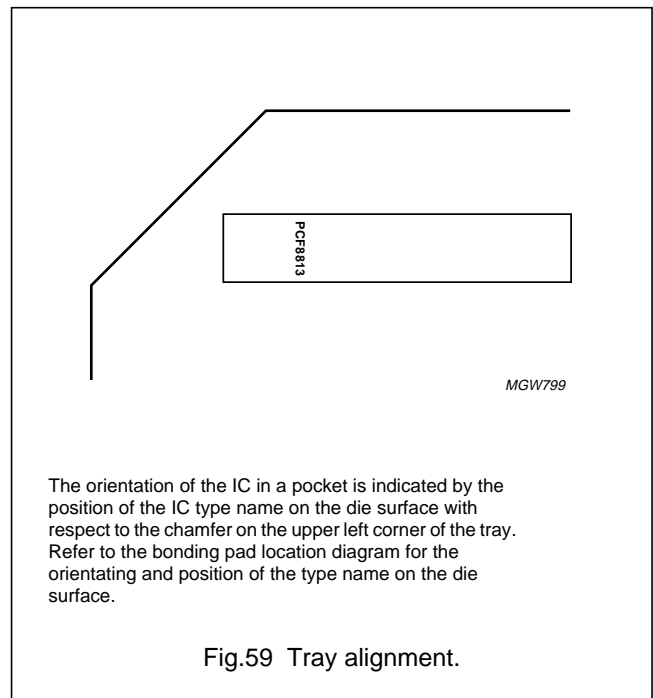


Table 29 Tray dimensions

| DIMS | DESCRIPTION | VALUE |
|------|--|----------|
| A | pocket pitch; x direction | 14.66 mm |
| B | pocket pitch; y direction | 3.76 mm |
| C | pocket width; x direction | 10.95 mm |
| D | pocket width; y direction | 1.95 mm |
| E | tray width; x direction | 50.8 mm |
| F | tray width; y direction | 50.8 mm |
| G | distance from cut corner to pocket (1, 1) centre | 10.74 mm |
| H | distance from cut corner to pocket (1, 1) centre | 4.72 mm |
| J | tray thickness | 3.96 mm |
| K | tray cross section | 1.78 mm |
| L | tray cross section | 2.44 mm |
| M | pocket depth | 0.89 mm |
| x | number of pockets in x direction | 3 |
| y | number of pockets in y direction | 12 |



(67 + 1) × 102 pixels matrix LCD driver**PCF8813****22 DATA SHEET STATUS**

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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(67 + 1) × 102 pixels matrix LCD driver**PCF8813**

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